EM88F712N

8-Bit Microprocessor

Product Specification

DOC. VERSION 1.6

ELAN MICROELECTRONICS CORP.
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APPENDIX

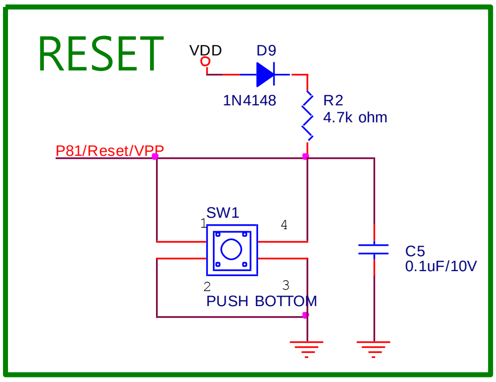
Specification Revision History

Doc. Version	Revision Description	Date
1.0	Initial released version	2017/07/20
1.1	1. Modified Drift Rate of Main oscillator 2. Modified Instruction Set 3. Modified DC Characteristics 4. Added note of programing IC	2017/11/16
1.2	1. Modified Figure 5-1 2. Modified description of R1 3. Modified Figure 6-2 4. Modified description of R33	2018/03/19
1.3	1. Modified Pin Description 2. Modified description of R46 3. Modified description of Register 4. Modified description of I/O Ports 5. Modified description of PWM	2018/07/06
1.4	1. Modified Pin Description 2. Modified Quality Assurance and Reliability table	2018/12/06
1.5	1. Added new package 2. Modified Description of Features 3. Modified Description of Register 4. Modified Description of Package table	2019/06/05
1.6	1. Modified Quality Assurance and Reliability	2020/11/26

User Application Note

(Before using this chip, take a look at the following description note, for it includes important messages.)

1. We strongly recommend that you place the following circuits on the reset pin, regardless of pin function. Its purpose is to prevent floating and burning when the high voltage backflush.



2. The value in the dead-time register must be less than the value in the duty cycle register in order to prevent unexpected behavior on both of the PWM outputs.

3. The PWM output will not be set, if the duty cycle is “0”

4. During ADC conversion, do not perform output instruction to maintain pins’ precision. In order to obtain accurate values, it is necessary to avoid any data transition on I/O pins during AD conversion.

5. Order of ADC Programming
   - Before setting the AD conversion pins (ADER1~2), the corresponding input channel (ADISR) and ADC power supply (ADP = 1) must be set.
   - After the AD conversion is completed, turn off the AD conversion pin function (ADER1~2).

6. AD pins that are not data-converted must be set as high-impedance input pins.

7. When programming EM88F712N (ED712N), the VDD must be 5V for the programming to be successful. Therefore, during EM88F712N programming and ED712N simulation, pay attention to the resistance of the surrounding components.

1 General Description

The EM88F712N is an 8-bit microprocessor designed and developed with low-power, high-speed CMOS technology. It is used to simulate the kernel: 2K*16-bits programmable ROM. This specification is used for 16 bits kernel simulation.

2 Features

- CPU configuration
  - Support 2K×16 bits program ROM
    *Endurance : 1000 cycles
  - (48+128) bytes general purpose register
  - 8 level stacks for subroutine nesting
  - Typically 1 μA during sleep mode
  - 3 programmable Level Volt Reset
    LVR: 2.3V/ 2.5V, 3.3V/ 3.5V, 3.8V/ 4.0V
  - 16 programmable Level Voltage Detectors
    HLVD: 2.2V, 2.3V, 2.4V, 2.5V, 2.6V,2.8V,2.9V, 3.1V, 3.3V,3.5V, 3.7V, 3.9V, 4.1V, 4.3V, 4.5V, 4.7V
  - Four CPU operation modes (Normal, Sleep, Green, Idle)
- I/O port configuration
  - 3 bidirectional I/O ports: P5, P6, P8
  - 3 programmable pin change wake-up ports: P5, P6, P8
  - 3 programmable pull-down I/O ports: P5, P6, P8
  - 3 programmable pull-high I/O ports: P5, P6, P8
  - 3 programmable open-drain I/O ports: P5, P6, P8
  - 3 programmable high-sink/drive I/O ports: P5, P6, P8
  - 4 external interrupt pins
- Operating voltage range:
  - 2.2V~5.5V at -40°C~85°C (industrial)
- Operating frequency range (based on 2 clocks):

Main oscillator:

- Crystal mode:
  DC ~ 20MHz at 4.5V~5.5V; DC ~ 12MHz at 3V~5.5V; DC ~ 8MHz at 2.2V~5.5V
- IRC mode:
  DC ~ 20MHz at 4.5V~5.5V; DC ~ 12MHz at 3V~5.5V; DC ~ 8MHz at 2.2~5.5V V

Internal RC Frequency	Drift Rate= Temperature (-40℃~+85℃)+ Voltage (2.2V~5.5V) (IRCPSS =0) + Process	
	NUWTR Total	UWTR Total
1MHz	±4%	±5%
4MHz	±4%	±5%
8MHz	±4%	±5%
10MHz	±4%	±5%
12MHz	±4%	±5%
16MHz	±4%	±5%
20MHz	±4%	±5%

Sub-oscillator:

- IRC mode: 16k/128k

- Peripheral configuration
  - 12+2 channels Analog-to-Digital Converter with 12-bit resolution + 1 internal reference for Vref+
  - 8-bit timers (TC1) with six modes including Timer, Counter, window, buzzer, PWM and PDO (programmable divider output) mode, respectively.
  - Two sets of complementary PWM, /PWM
  - Comparator/OP internal reference
  - Universal asynchronous receiver / transmitter (UART) available
  - Serial transmitter/receiver interface (SPI): three wire synchronous communication
  - Power-down (Sleep) mode
  - High EFT immunity
- 15 available interrupts (4 external, 11 internal)
  - 4 external interrupts
  - Input-port status changed interrupt (wake up from sleep mode)
  - comparator interrupts
  - HLVD interrupt
  - Timer interrupt
  - Two complementary PWM
  - ADC completion interrupt
  - UART TX, RX, RX error interrupt
  - SPI interrupt
- Package Type:
  - 20 pin SOP 300mil : EM88F712NSO20
  - 20 pin SSOP 209mil : EM88F712NSS20
  - 20 pin SSOP 150mil : EM88F712NSS20A
  - 16 pin SOP 150mil : EM88F712NSO16A
  - 16 pin SSOP 150mil : EM88F712NSS16

Note: These are Green Products which do not contain hazardous substances.

- 99.9% single instruction cycle commands

3 Pin Configuration (Package)

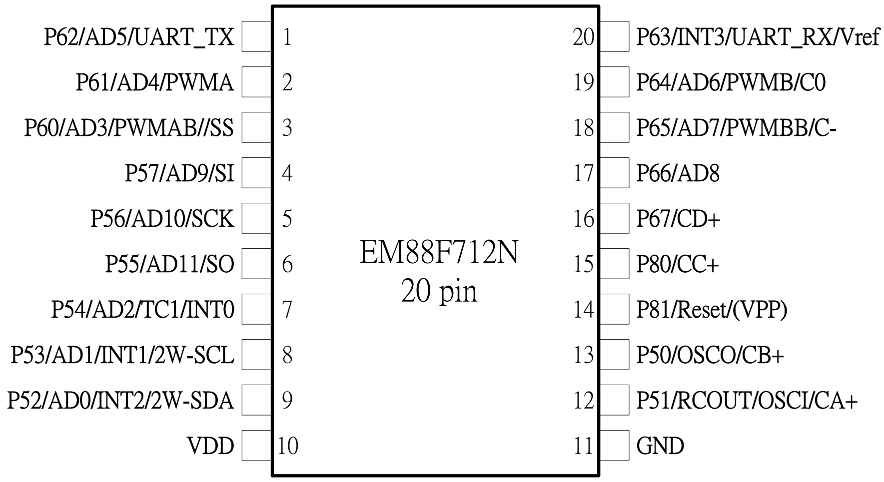


Figure 3-1 EM88F712NSO20/SS20/SS20A

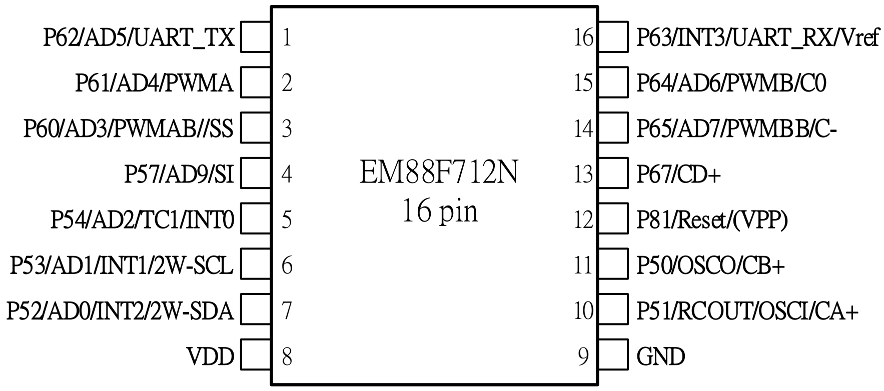


Figure 3-3 EM88F712NSO16A/SS16

4 Pin Description

Table 1 EM88F712N Pin Description

Legend: ***ST:*** *Schmitt Trigger input* ***AN:*** *Analog pin*
CMOS: *CMOS output* ***XTAL:*** *Oscillation pin for crystal/resonator*

Name	Function	Input Type	Output Type	Description
P50/OSCO/CB+	P50	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	OSCO	–	XTAL	Clock output from crystal oscillator
	CB+	AN	–	Non-inverting end of Comparator/OP
P51/OSCI/RCOUT/CA+	P51	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	OSCI	XTAL	–	External clock crystal resonator oscillator input pin
	RCOUT	–	CMOS	Clock output of internal RC oscillator Clock output of external RC oscillator (open-drain)
	CA+	AN	–	OP/CMP non-inverting input
P52/AD0/INT2/2W-SDA	P52	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	AD0	AN	–	ADC Input 0
	INT2	ST	–	External interrupt pin
	(2W-SDA)	ST	CMOS	DATA pin for Writer programming
P53/AD1/INT1/2W-SCL	P53	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	AD1	AN	–	ADC Input 1
	INT1	ST	–	External interrupt pin
	(2W-SCL)	ST	–	CLOCK pin for Writer programming
P54/AD2/TC1/INT0	P54	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	AD2	AN	–	ADC Input 2
	TC1	ST	CMOS	Timer 1 input (Counter/Capture/Window) Timer 1 output (PDO/PWM/Buzzer)
	INT0	ST	–	External interrupt pin
P55/AD11/SO	P55	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	AD11	AN	–	ADC Input 11
	SO	–	CMOS	SPI serial data output
P56/AD10/SCK	P56	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	AD10	AN	–	ADC Input 10
	SCK	ST	CMOS	SPI serial clock input/output

(Continuation)

Name	Function	Input Type	Output Type	Description
P57/AD9/SI	P57	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	AD9	AN	–	ADC Input 9
	SI	ST	–	SPI serial data input
P60/AD3/PWMAB//SS	P60	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	AD3	AN	–	ADC Input 3
	PWMAB	–	CMOS	PWMAB output
	/SS	ST	–	SPI slave select pin
P61/AD4/PWMA	P61	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	AD4	AN	–	ADC Input 4
	PWMA	–	CMOS	PWMA output
P62/AD5/UART_TX	P62	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	AD5	AN	–	ADC Input 5
	TX	ST	–	UART TX input
P63/INT3/UART_RX/Vref	P63	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	INT3	ST	–	External interrupt pin
	RX	ST	–	UART RX input
	Vref	AN		Voltage reference for ADC
P64/AD6/PWMB/CO	P64	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	AD6	AN	–	ADC Input 6
	PWMB	–	CMOS	PWMB output
	CO	–	CMOS	Output of Comparator/OP
P65/AD7/PWMBB/C-	P65	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	AD7	AN	–	ADC Input 7
	PWMBB	–	CMOS	PWMBB output
	C-	AN		Inverting end of Comparator/OP
P66/AD8	P66	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	AD8	AN	–	ADC Input 8
P67/CD+	P67	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	CD+	AN	–	Non-inverting end of Comparator/OP

(Continuation)

Name	Function	Input Type	Output Type	Description
P80/CC+	P80	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	CC+	AN	–	Non-inverting end of Comparator/OP
P81//Reset/ **(VPP)**	P81	ST	CMOS	Bidirectional I/O pin with programmable It is open-drain
	/RESET	ST	-	Reset pin. It is open-drain
	(VPP)	Power	-	VPP pin for Writer programming
VDD **(VDD)**	VDD	Power	–	Power
	VDD	Power	–	VDD for Writer programming
VSS **(VSS)**	VSS	Power	–	Ground
	VSS	Power	–	VSS for Writer programming

Pin control condition repeat function starting capability

Pin Function	I/O Status		Pin Control		
	I/O Direction	Pin Change WK/Int.	Pull High	Pull Low	O.D.
General Input	Input	S/W	S/W	S/W	S/W
General Output	Output	Disable	S/W	S/W	S/W
PWM	Output	Disable	S/W	S/W	S/W
TC-IN	Input	Disable	S/W	S/W	S/W
TC-OUT	Output	Disable	S/W	S/W	S/W
RSTB (VPP pin)	Input	Disable	–	S/W	S/W
EX_INT	Input	Disable	S/W	S/W	S/W
SPI-SDI	Input	Disable	S/W	S/W	S/W
SPI-SDO	Output	Disable	S/W	S/W	S/W
SPI-SCK-IN	Input	Disable	S/W	S/W	S/W
SPI-SCK-OUT	Output	Disable	S/W	S/W	S/W
UART-TX	Output	Disable	S/W	S/W	S/W
UART-RX	Input	Disable	S/W	S/W	S/W
AD	Input	Disable	Disable	Disable	S/W
OP/VO	Input	Disable	Disable	Disable	S/W
CMP/IN	Input	Disable	Disable	Disable	S/W
CMP/CO	Output	Disable	Disable	Disable	S/W
OSCI	Input	Disable	Disable	Disable	S/W
OSCO	Input	Disable	Disable	Disable	S/W

Disable → forced to shut off

Enable → forced to open

S/W → The initial value in the control register is set as "Disable".

Notes:

1. For non-I/O function, the Pin Change Wake-up/Interrupt function should be disabled.
2. Priority: INMODE PIN > Analog function > Digital Function > General I/O Function

5 System Overview

5.1 Memory Map

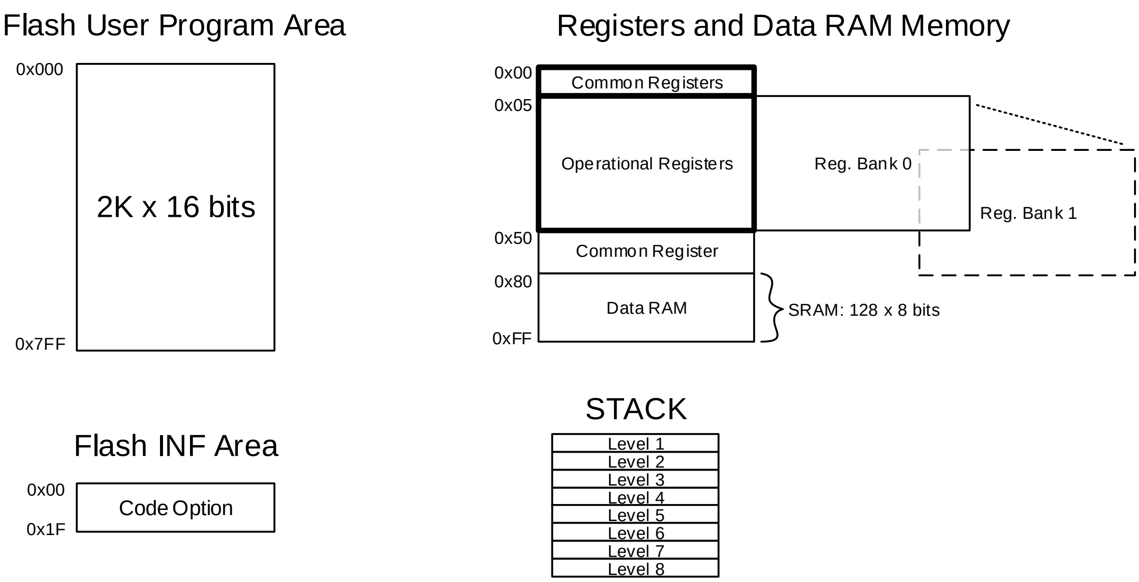


Figure 5-1 Memory Map

Notes:

1. Flash User Program Area is protected when power down occurs, and will not be read, written and erased from the OCDS.

5.2 Block Diagram

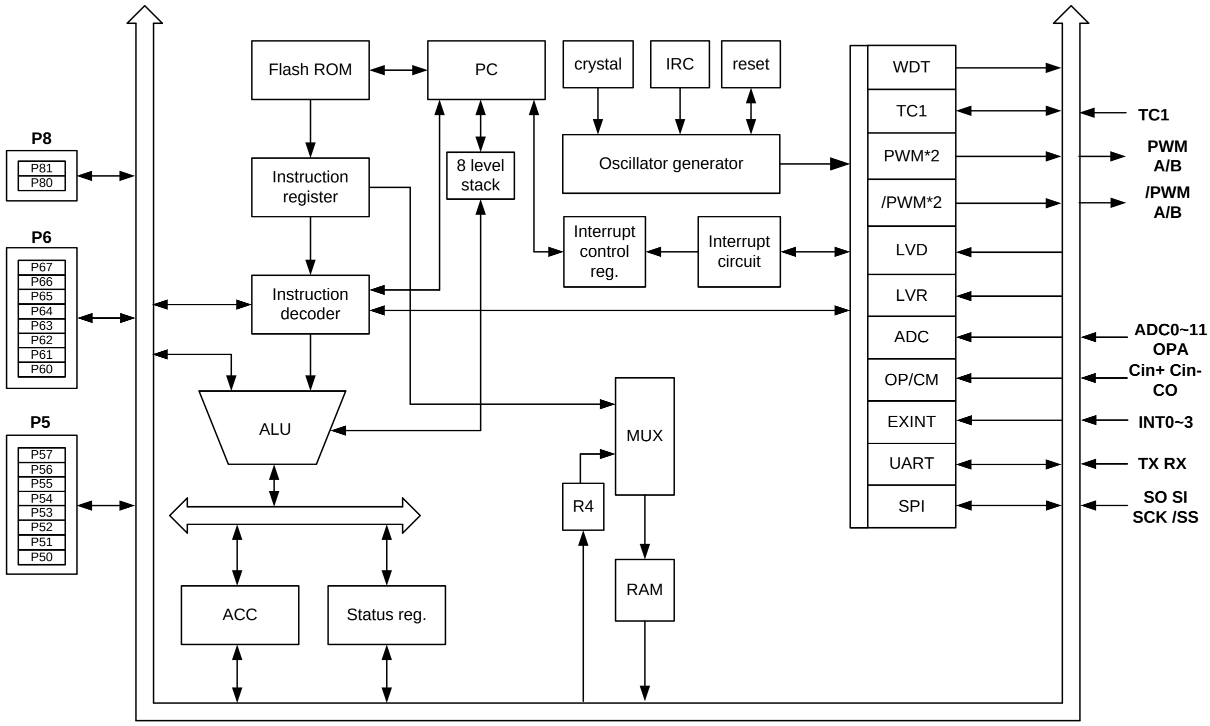


Figure 5-2 Functional Block Diagram

6 Functional Description

6.1 Operational Registers

6.1.1 R0 IAR (Indirect Addressing Register)

R0 is not a physically implemented register. Its major function is to perform as an indirect addressing pointer. Any instruction using R0 as a pointer actually accesses data pointed by the RAM Select Register (R4).

6.1.2 R1 BSR (Bank Selection Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	SBS0	–	–	–	–
–	–	–	R/W	–	–	–	–

Bits 7~5: Not used, set to “0” all the time.

Bit 4 (SBS0): Special register bank select bit. It is used to select Bank 0/1 of Special Registers **R5~R4F**.

0: Bank 0

1: Bank 1

Bits 3~0: Not used, set to "0" all the time.

6.1.3 R2 PCL (Program Counter Low)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (PC7~PC0): Low byte of program counter.

- Depending on device type, R2 and hardware stack are **16**-bit wide. The structure is depicted in Figure 3.
- Generate 2**K**×**16** bits on-chip Flash ROM addresses to the relative programming instruction codes. One program page is **2048** words long.
- R2 is set as all "0"s when under RESET condition.
- "JMP" instruction allows direct loading of the lower **12** program counter bits. Thus, "JMP" allows PC to go to any location within a page.

- "CALL" instruction loads the lower **12** bits of the PC, and the present PC value will add 1 and is pushed into the stack. Thus, the subroutine entry address can be located anywhere within a page.
- "RET" ("RETL k", "RETI") instruction loads the program counter with the contents of the top-level stack.
- "ADD R2, A" allows a relative address to be added to the current PC, and the ninth and above bits of the PC will increase progressively.
- "MOV R2, A" allows the loading of an address from the "A" register to the lower 8 bits of the PC, and the ninth and above bits of the PC will not be changed.
- Any instruction except “ADD R2, A” that is written to R2 (e.g. "MOV R2, A", "BC R2, 6", etc.) will cause the ninth bit and the above bits (A8~A12) of the PC not to change.

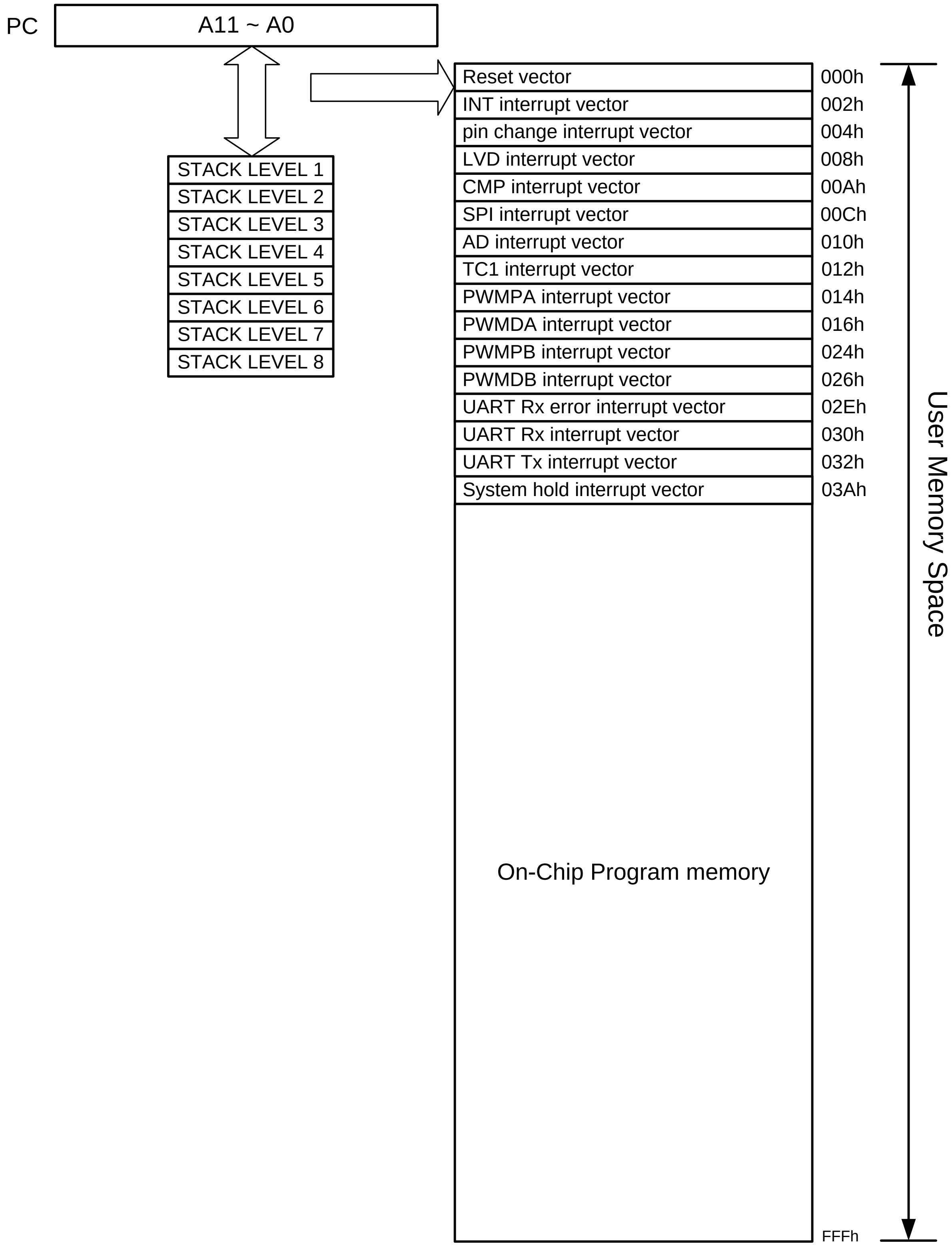


Figure 6-1 Program Counter Organization

■ Data Memory Configuration

Address	Bank 0	Bank 1
0X00	IAR (Indirect Addressing Register)	–
0X01	BSR (Bank Select Control Register)	
0X02	PC (Program Counter)	
0X03	SR (Status Register)	
0X04	RSR (RAM Select Register)	
0X05	Port 5	IOCR8
0X06	Port 6	Unused
0X07	Unused	Unused
0X08	Port 8	P5PHCR
0X09	Unused	P6PHCR
0X0A	Unused	P8PHCR
0x0B	IOCR5	P5PLCR
0X0C	IOCR6	P6PLCR
0X0D	Unused	P8PLCR
0X0E	OMCR (Operating Mode Control Reg.)	P5HDSCR
0X0F	EIESCR (External Interrupt Edge Selection Control Reg.)	P6HDSCR
0X10	WUCR1	P8HDSCR
0X11	WUCR2	P5ODCR
0X12	WUCR3	P6ODCR
0X13	Unused	P8ODCR
0X14	SFR1 (Status Flag Reg. 1)	DeadTCR
0X15	SFR2 (Status Flag Reg. 2)	DeadTR
0X16	SFR3 (Status Flag Reg. 3)	PWMSCR
0X17	SFR4 (Status Flag Reg. 4)	PWMACR
0X18	SFR5 (Status Flag Reg. 5)	PRDAL
0X19	SFR6 (Status Flag Reg. 6)	PRDAH
0X1A	Unused	DTAL
0X1B	IMR1 (Interrupt Mask Reg. 1)	DTAH
0X1C	IMR2 (Interrupt Mask Reg. 2)	TMRAL
0X1D	IMR3 (Interrupt Mask Reg. 3)	TMRAH
0X1E	IMR4 (Interrupt Mask Reg. 4)	PWMBCR
0X1F	IMR5 (Interrupt Mask Reg. 5)	PRDBL
0X20	IMR6 (Interrupt Mask Reg. 6)	PRDBH
0X21	WDTCR	DTBL

Address	Bank 0	Bank 1
0X22	Unused	DTBH
0X23	Unused	TMRBL
0X24	TC1CR1	TMRBH
0X25	TC1CR2	Unused
0X26	TC1DA	Unused
0X27	TC1DB	Unused
0X28	Unused	Unused
0X29	Unused	Unused
0X2A	Unused	Unused
0x2B	Unused	Unused
0X2C	Unused	Unused
0X2D	Unused	Unused
0X2E	Unused	Unused
0X2F	Unused	Unused
0X30	Unused	Unused
0X31	Unused	Unused
0X32	Unused	Unused
0X33	Unused	URCR
0X34	Unused	URS
0X35	Unused	URTD
0X36	SPICR	URRDL
0X37	SPIS	URRDH
0X38	SPIR	Unused
0X39	SPIW	Unused
0X3A	CMP1CR	Unused
0x3B	Unused	Unused
0X3C	Unused	Unused
0X3D	Unused	Unused
0X3E	ADCR1	Unused
0X3F	ADCR2	Unused
0X40	ADISR	Unused
0X41	ADER1	Unused
0X42	ADER2	Unused
0X43	ADDL	Unused

Address	Bank 0	Bank 1
0X44	ADDH	Unused
0X45	ADCVL	Unused
0X46	ADCVH	Unused
0X47	Unused	STKMON
0X48	Unused	PCH
0X49	Unused	HLVDCR
0X4A	Unused	Unused
0x4B	Unused	Unused
0X4C	Unused	Unused
0X4D	Unused	Unused
0X4E	Unused	Unused
0X4F	Unused	Unused
0X50	General Purpose Register	
0X51		
:		
:		
0X7F		
0X80	Bank 0	
0X81		
:		
:		
:		
0XFE		
0XFF		

Figure 6-2 Data Memory Configuration

6.1.4 R3 SR (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INT	N	OV	T	P	Z	DC	C
F	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (INT): Interrupt Enable flag

0: Interrupt masked by DISI or hardware interrupt

1: Interrupt enabled by ENI/DISI instructions

Bit 6 (N): Negative flag

The negative flag stores the state of the most significant bit of the output result

0: The result of the operation is not negative

1: The result of the operation is negative

Bit 5 (OV): Overflow flag.

OV is set when a two-complement overflow occurs as a result of an operation

0: No overflow occurs

1: Overflow occurs

Bit 4 (T): Time-out bit.

Set to 1 with the "SLEP" and "WDTC" commands, or during power-up and reset to “0” by WDT time-out.

Bit 3 (P): Power down bit.

Set to ”1” during power-on or by a "WDTC" command and reset to ”0” by a "SLEP" command.

Bit 2 (Z): Zero flag.

Set to "1" if the result of an arithmetic or logic operation is zero.

Bit 1 (DC): Auxiliary carry flag

Bit 0 (C): Carry flag

6.1.5 R4 RSR (RAM Select Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RSR7	RSR6	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (RSR7~RSR0): These bits are used to select registers (Address: 00~FF) in indirect addressing mode. For more details, refer to Figure 6-2 *Data Memory Configuration*.

6.1.6 Bank 0 R5 ~ R8 Port 5 ~ Port 8

R5, R6, R7, R8, R9 and RA are I/O data registers.

6.1.7 Bank 0 RB~RC IOCR5 ~ IOCR6

These registers are used to control the I/O port direction. They are both readable and writable.

0: Put the relative I/O pin as output

1: Put the relative I/O pin into high impedance (input)

6.1.8 Bank 0 RE OMCR (Operating Mode Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CPUS	IDLE	–	IIPS	FMSF	RCM2	RCM1	RCM0
R/W	R/W	0	R/W	R	R/W	R/W	R/W

Bit 7 (CPUS): CPU Oscillator Source Select.

0: Fs: sub-oscillator

1: Fm: main-oscillator

When CPUS=0, the CPU oscillator selects the sub-oscillator and the main oscillator is stopped.

Bit 6 (IDLE): Idle Mode Enable Bit. This bit will determine as to which mode to go to or be activated after SLEP instruction.

0: "IDLE=0"+SLEP instruction → sleep mode

1: "IDLE=1"+SLEP instruction → idle mode

Bits 5: This bit always fixed 0.

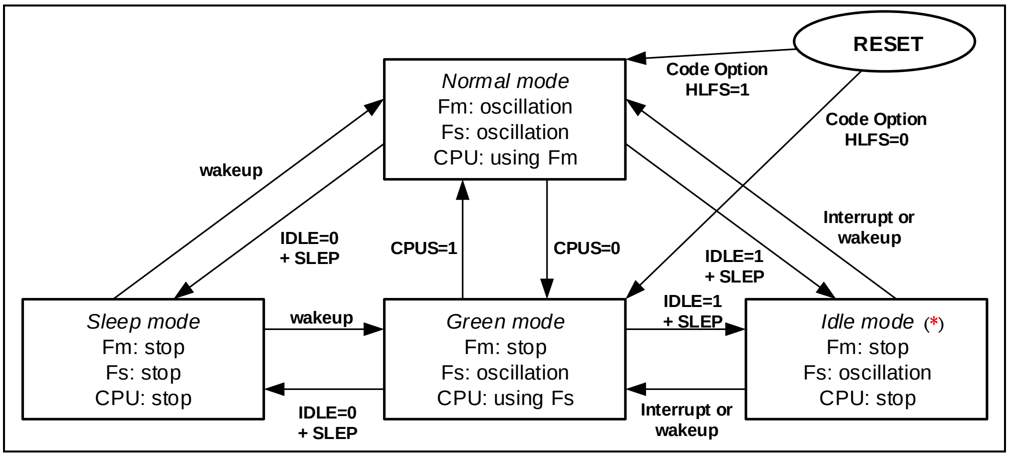


Figure 1.CPU operation mode

Note

(*) Switching Operation Mode from Idle → Normal, Idle → Green

If the clock source of the timer is Fs, the timer/counter will continue to count in Idle mode. When the matching condition of the timer/counter occurs during Idle mode, the interrupt flag of the timer/counter will be active. The MCU will jump to the interrupt vector when the corresponding interrupt is enabled.

HLFS = 0 (Normal)

Fmain	Fsub	Power-on LVR	Pin-Reset / WDT	
			N / G / I	S
RC 1M, 4M, 8M, 10M	RC	16ms + WSTO + 8*1/Fmain	WSTO + 8*1/Fmain	WSTO + 8*1/Fmain
RC 12M,16M, 20M	RC	16ms + WSTO +16*1/Fmain	WSTO + 16*1/Fmain	WSTO + 16*1/Fmain
XT	RC	16ms + WSTO +510*1/Fmain	WSTO + 510*1/Fmain	WSTO + 510*1/Fmain

HLFS = 1 (Green)

Fmain	Fsub	Power-on LVR	Pin-Reset / WDT	
			N / G / I	S
RC 1M, 4M, 8M, 10M,12M, 16M, 20M	RC	16ms + WSTO + 1 *1/Fsub	WSTO + 1*1/Fsub	WSTO + 1*1/Fsub
XT	RC	16ms + WSTO + 1*1/Fsub	WSTO + 1*1/Fsub	WSTO + 1*1/Fsub

Fmain	Fsub	G → N	I → N	S → N
RC 1M, 4M, 8M, 10M	RC	WSTO + 8*1/Fmain	WSTO + 8*1/Fmain	WSTO + 8*1/Fmain
RC 12M,16M, 20M	RC	WSTO + 16*1/Fmain	WSTO + 16*1/Fmain	WSTO + 16*1/Fmain
XT	RC	WSTO + 510*1/Fmain	WSTO + 510*1/Fmain	WSTO + 510*1/Fmain

Fmain	Fsub	I → G	S → G
RC XT	RC	WSTO + 1*1/Fsub	WSTO + 1*1/Fsub

N: Normal mode WSTO: Waiting Time from Start-to-Oscillation
G: Green mode I: Idle mode S: Sleep mode

Bit 4 (IIPS): IRC Internal power switch bit. Used in mode change. (when IRC PSS is set to “1”).

0: Internal power supply on, high power consumption but short starting time.

1: Internal power off, low power consumption but long start-up time.

Bit 3 (FMSF): Fm Stable Flag bit.

0: Indicate that the frequency is unstable.

1: Indicate that the frequency has stabilized.

Bits 2~0 (RCM2~RCM0): Internal RC mode select bits

RCM2	RCM1	RCM0	Frequency (MHz)
0	0	0	4 (Default)
0	0	1	1
0	1	0	8
0	1	1	10
1	0	0	12
1	0	1	16
1	1	0	20
1	1	1	Reserved

6.1.9 Bank 0 RF EIESCR (External Interrupt Edge Select Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	EI32ES1	EI32ES0	EI1ES1	EI1ES0	EI0ES1	EI0ES0
–	–	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~6: Not used, set to “0” all the time

Bit 5~0 (EIxES1~0): External interrupt edge select bit

EIxES1	EIxES0	Interrupt Edge Select
0	0	Falling edge interrupt
0	1	Rising edge interrupt
1	×	Falling and Rising edge interrupts

6.1.10 Bank 0 R10 WUCR1 (Wake-up Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	CMPWK	HLVDWK	ADWK	INTWK1	INTWK0	–	–
–	R/W	R/W	R/W	R/W	R/W	–	–

Bit 7: Not used, set to “0” all the time

Bit 6 (CMPWK): Comparator Wake-up Enable Bit

0: Disable comparator wake-up.

1: Enable comparator wake-up.

Bit 5 (HLVDWK): High/Low Voltage Detect Wake-up Enable Bit

0: Disable High / Low Voltage Detect wake-up.

1: Enable High / Low Voltage Detect wake-up.

Bit 4 (ADWK): A/D Converter Wake-up Function Enable Bit

0: Disable AD converter wake-up

1: Enable AD converter wake-up

When the AD Complete status is used to enter an interrupt vector or to wake up the IC from sleep/idle mode with AD conversion running, the ADWK bit must be set to "Enable".

Bits 3~2 (INTWK1~0): External Interrupt (INT pin) Wake-up Function Enable Bit

0: Disable external interrupt wake-up

1: Enable external interrupt wake-up

When the External Interrupt status changed is used to enter an interrupt vector or to wake up the IC from sleep/idle mode, the INTWK bits must be set to "Enable".

Bits 1~0: Not used, set to "0" all the time

6.1.11 Bank 0 R11 WUCR2 (Wake-up Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	–	SPIWK		–	–
–	–	–	–	R/W		–	–

Bits 7~4: Not used, set to "0" all the time.

Bit 3 (SPIWK): SPI wake-up enable bit. Functions when SPI works in Slave mode.

0: Disable SPI wake-up

1: Enable SPI wake-up

Bits 2~0: Not used, set to "0" all the time

6.1.12 Bank 0 R12 WUCR3 (Wake-up Control Register 3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ICWKP8		ICWKP6	ICWKP5				INTWK32
R/W		R/W	R/W				R/W

Bits 7, 5~4 (ICWKP8,6~5): (Port 8, 6~5) Pin-change Wake-up Function Enable Bit

0: Disable pin change wake-up function

1: Enable pin change wake-up function

Bit 6: Not used, set to "0" all the time

Bit 3~1: Not used, set to "0" all the time

Bits 0 (INTWK7~2): External Interrupt (INT pin) Wake-up Function Enable Bit

0: Disable external interrupt wake-up

1: Enable external interrupt wake-up

When the External Interrupt status change is used to enter an interrupt vector or to wake up the IC from sleep/idle mode, the INTWK bits must be set to "Enable".

6.1.13 Bank 0 R14 SFR1 (Status Flag Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
−	CMPSF	HLVDSF	ADSF	EXSF1	EXSF0	−	−
−	F	F	F	F	F	−	−

Each corresponding status flag is set to **"1"** when interrupt condition is triggered.

Bit 7: Not used, set to "0" all the time.

Bit 6 (CMPSF): Comparator status flag. Set when a change occurs in the output of Comparator, reset by software.

Bit 5 (HLVDSF): High/Low Voltage Detector status flag.

HLVDEN	HLVDS3~0	HLVD Voltage Interrupt Level	HLVDSF
1	1111	4.7V	1*
1	.	.	1*
1	.	.	1*
1	0000	2.2V	1*
0	xxxx	NA	0

Bit 4 (ADSF): Status flag for Analog-to-Digital conversion. Set when AD conversion is completed, reset by software.

Bits 3~2 (EXSF1~0): External interrupt status flag.
Bit 1: Not used, set to "0" all the time

NOTE
If a function is enabled, the corresponding status flag would be active whether the interrupt mask is enabled or not.

6.1.14 Bank 0 R15 SFR2 (Status Flag Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
−	−	UERRSF	URSF	UTSF			TC1DASF
−	−	F	F	F			F

Each corresponding status flag is set to **"1"** when interrupt condition is triggered.

Bits 7~6: Not used, set to "0" all the time

Bit 5 (UERRSF): UART error-receiving Status flag. This flag is cleared by software or when UART is disabled.

Bit 4 (URSF): UART receive mode data buffer full Status flag. This flag is cleared by software.

Bit 3 (UTSF): UART transmit mode data buffer empty flag. This flag is cleared by software.

Bits 2~1: Not used, set to "0" all the time

Bit 0 (TC1DASF): TC1DA matches Status flag. This flag is cleared by software.

6.1.15 Bank 0 R16 SFR3 (Status Flag Register 3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
				PWMBPSF	PWMBDSF	PWMAPSF	PWMADSF
		F	F	F	F	F	F

Bits 7~4: Not used, set to "0" all the time

Bit 3 (PWMBPSF): Status flag of period-matching for PWMB (Pulse Width Modulation). Set when a selected period is reached, reset by software.

Bit 2 (PWMBDSF): Status flag of duty-matching for PWMB (Pulse Width Modulation). Set when a selected duty is reached, reset by software.

Bit 1 (PWMAPSF): Status flag of period-matching for PWMA (Pulse Width Modulation). Set when a selected period is reached, reset by software.

Bit 0 (PWMADSF): Status flag of duty-matching for PWMA (Pulse Width Modulation). Set when a selected duty is reached, reset by software.

NOTE

If a function is enabled, the corresponding status flag would be active whether the interrupt mask is enabled or not.

6.1.16 Bank 0 R17 SFR4 (Status Flag Register 4)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P8ICSF		P6ICSF	P5ICSF	SPISF			
F		F	F	F			

Bit 7 (P8ICSF): Port 8 Status flag. This flag is cleared by software.

Bits 6: Not used, set to "0" all the time

Bit 5 (P6ICSF): Port 6 Status flag. This flag is cleared by software.

Bit 4 (P5ICSF): Port 5 Status flag. This Flag is cleared by software.

Bit 3 (SPISF): SPI mode Status flag. This flag is cleared by software.

Bits 2~0: Not used, set to "0" all the time

> **NOTE**
> *If a function is enabled, the corresponding Status flag would be active whether the interrupt mask is enabled or not.*

6.1.17 Bank 0 R18 SFR5 (Status Flag Register 5)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
						EXSF3	EXSF2
						F	F

Each corresponding Status flag is set to **"1"** when interrupt condition is triggered.

Bits 7~2: Not used, set to "0" all the time

Bits 1~0 (EXSF3~2): External interrupt status flag.

> **NOTE**
> *If a function is enabled, the corresponding status flag would be active regardless whether the interrupt mask is enabled or not.*

6.1.18 Bank 0 R19 SFR6 (Status Flag Register 6)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SHSF							TC1DBSF
F							F

Each corresponding status flag is set to "1" when interrupt condition is triggered.

Bit 7 (SHSF): System hold status flag. Set when system hold occurs, reset by software.

Bits 6~1: Not used, set to "0" all the time

Bit 0 (TC1DBSF): TC1DB matches status flag, cleared by software.

> **NOTE**
> *If a function is enabled, the corresponding status flag would be active regardless whether the interrupt mask is enabled or not.*

6.1.19 Bank0 R1A: Reserved

6.1.20 Bank 0 R1B IMR1 (Interrupt Mask Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
−	CMPIE	HLVDIE	ADIE	EXIE1	EXIE0	−	−
−	R/W	R/W	R/W	R/W	R/W	−	−

Bits 7~6: Not used, set to "0" all the time.

Bit 6 (CMPIE): CMPSF interrupt enable bit.

0: Disable CMPSF interrupt

1: Enable CMPSF interrupt

When Comparator output status changes is used to enter interrupt vector, the CMPIE bit must be set to "enable".

Bit 5 (HLVDIE): HLVDSF interrupt enable bit.

0: Disable HLVDSF interrupt

1: Enable HLVDSF interrupt

Bit 4 (ADIE): ADSF interrupt enable bit.

0: Disable ADSF interrupt

1: Enable ADSF interrupt

Bit 3 (EXIE1): EXSF1 interrupt enable bit and /INT1 function enable bit.

0: Disable EXSF1 interrupt

1: Enable EXSF1 interrupt

Bit 2 (EXIE0): EXSF0 interrupt enable bit and /INT0 function enable bit.

0: Disable EXSF0 interrupt

1: Enable EXSF0 interrupt

Bit 1~0: Not used, set to "0" all the time

> **NOTE**
> *If the interrupt mask and instruction "ENI" are enabled, the program counter would jump into the corresponding interrupt vector when the corresponding status flag is set.*

6.1.21 Bank 0 R1C IMR2 (Interrupt Mask Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
−	−	UERRIE	URIE	UTIE	−	−	TC1IE
−	−	R/W	R/W	R/W	−	−	R/W

Bits 7~6: Not used, set to "0" all the time.

Bit 5 (UERRIE): UART receive error interrupt enable bit.

0: Disable UERRSF interrupt

1: Enable UERRSF interrupt

Bit 4 (URIE): UART receive mode Interrupt enable bit.

0: Disable URSF interrupt

1: Enable URSF interrupt

Bit 3 (UTIE): UART transmit mode interrupt enable bit.

0: Disable UTSF interrupt

1: Enable UTSF interrupt

Bits 2~1: Not used, set to “0” all the time.

Bit 0 (TC1IE): Interrupt enable bit.

0: Disable TC1DASF and TC1DBSF interrupt

1: Enable TC1DASF and TC1DBSF interrupt

> **NOTE**
> *If the interrupt mask and instruction “ENI” are enabled, the program counter would jump to the corresponding interrupt vector when the corresponding status flag is set.*

6.1.22 Bank 0 R1D IMR3 (Interrupt Mask Register 3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
				PWMBPIE	PWMBDIE	PWMAPIE	PWMADIE
				R/W	R/W	R/W	R/W

Bits 7~4: Not used, set to "0" all the time

Bit 3 (PWMBPIE): PWMBPSF interrupt enable bit.

0: Disable period-matching of PWMB interrupt

1: Enable period-matching of PWMB interrupt

Bit 2 (PWMBDIE): PWMBDSF interrupt enable bit.

0: Disable duty-matching of PWMB interrupt

1: Enable duty-matching of PWMB interrupt

Bit 1 (PWMAPIE): PWMAPSF interrupt enable bit.

0: Disable period-matching of PWMA interrupt

1: Enable period-matching of PWMA interrupt

Bit 0 (PWMADIE): PWMADSF interrupt enable bit.

0: Disable duty-matching of PWMA interrupt

1: Enable duty-matching of PWMA interrupt

> **NOTE**
> *If the interrupt mask and instruction “ENI” are enabled, the program counter would jump into corresponding interrupt vector when the corresponding status flag is set.*

6.1.23 Bank 0 R1E IMR4 (Interrupt Mask Register 4)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P8ICIE		P6ICIE	P5ICIE	SPIIE			
R/W		R/W	R/W	R/W			

Bits 7 (P8ICIE): Ports 8 pin-change interrupt enable bit.

0: Disable P8ICSF interrupt

1: Enable P8ICSF interrupt

Bits 6: Not used, set to "0" all the time

Bits 5~4 (P6ICIE ~P5ICIE): Ports 6~5 pin-change interrupt enable bits.

0: Disable P6ICSF ~ P5ICSF interrupt

1: Enable P6ICSF ~ P5ICSF interrupt

Bit 3 (SPIIE): Interrupt enable bit.

0: Disable SPISF interrupt

1: Enable SPISF interrupt

Bits 2~0: Not used, set to "0" all the time

NOTE

If the interrupt mask and instruction "ENI" are enabled, the program counter would jump to the corresponding interrupt vector when the corresponding status flag is set.

6.1.24 Bank 0 R1F IMR5 (Interrupt Mask Register 5)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
						EXIE3	EXIE2
						R/W	R/W

Bits 7~2: Not used, set to "0" all the time

Bits 1~0 (EXIE3~2): EXSF3~2 interrupt enable bit.

0: Disable EXSF3~2 interrupt

1: Enable EXSF3~2 interrupt

INT Pin	Enable Condition	Edge	Digital Noise Reject
INTX	EXIEX	Rising or Falling	8/Fc or 32/Fc

NOTE

1. *The compound pin used as INT pin determines whether the interrupt mask is enabled or not.*
2. *If the interrupt mask and instruction "ENI" are enabled, the program counter would jump to the corresponding interrupt vector when the corresponding Status flag is set.*

6.1.25 Bank 0 R20 IMR6 (Interrupt Mask Register 6

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SHIE							
R/W							

Bit 7 (SHIE): SHSF Interrupt Enable Bit.

0: Disable SHSF interrupt

1: Enable SHSF interrupt

Bits 6~0: Not used, set to "0" all the time.

NOTE

If the interrupt mask and instruction "ENI" are enabled, the program counter would jump to the corresponding interrupt vector when the corresponding status flag is set.

6.1.26 Bank 0 R21 WDTCR (Watchdog Timer Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	FSSF	–	–	PSWE	WPSR2	WPSR1	WPSR0
R/W	R	–	–	R/W	R/W	R/W	R/W

Bit 7 (WDTE): Watchdog Timer Enable Bit. WDTE is both readable and writable.

0: Disable WDT

1: Enable WDT

Bit 6 (FSSF): Fs Stable Flag bit

0: Indicate that the frequency is unstable.

1: Indicate that the frequency has stabilized.

Bits 5~4: Not used, set to "0" all the time.

Bit 3 (PSWE): Prescaler enable bit for WDT

0: Prescaler disable bit. WDT rate is 1:1

1: Prescaler enable bit. WDT rate is set at Bits 2~0.

Bits 2~0 (WPSR2~ WPSR 0): WDT Prescaler Bits

WPSR2	WPSR1	WPSR0	WDT Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.1.27 Bank 0 R24 TC1CR1 (Timer/Counter 1 Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC1S	TC1RC	TC1SS1		TC1FF	TC1OMS	TC1IS1	TC1IS0
R/W	R/W	R/W		R/W	R/W	R/W	R/W

Bit 7 (TC1S): Timer/Counter 1 start control (main switch for all modes)

0: Stop and clear the counter (default)

1: Start Timer/Counter 1

Bit 6 (TC1RC): Timer 1 Read Control Bit

0: When this bit is set to "0", data from TC1DB cannot be read (default).

1: When this bit is set to "1", data is read from TC1DB. The read data is the enumerated counting number.

Bit 5 (TC1SS1): Timer/Counter 1 clock source select Bit 1

0: Select internal clock as counting source (Fc) Fs/Fm (default)

1: Select external TC1 pin as counting source (Fc). It is used only for timer/counter mode.

Bits 4: Not used, set to "0" all the time.

Bit 3 (TC1FF): Inversion for Timer/Counter 1 as PWM or PDO mode

0: Duty is Logic 1 (default)

1: Duty is Logic 0

Bit 2 (TC1OMS): Timer Output Mode Select Bit

0: Repeating mode (default)

1: One-shot mode

> **NOTE**
> *One-shot mode means the timer only counts a cycle.*

Bits 1~0 (TC1IS1~ TC1IS0): Timer 1 Interrupt Type Select Bits. These two bits are used when the Timer operates in Capture and PWM mode.

TC1IS1	TC1IS0	Timer 1 Interrupt Type Select
0	0	TC1DA (period) matching
0	1	TC1DB (duty) matching
1	×	TC1DA and TC1DB matching

6.1.28 Bank 0 R25 TC1CR2 (Timer/Counter 1 Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC1M2	TC1M1	TC1M0	TC1SS0	TC1CK3	TC1CK2	TC1CK1	TC1CK0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~5 (TC1M2~TC1M0): Timer/Counter 1 operation mode select.

TC1M2	TC1M1	TC1M0	Operating Mode Select
0	0	0	Timer/Counter Rising Edge
0	0	1	Timer/Counter Falling Edge
0	1	0	Capture Mode Rising Edge
0	1	1	Capture Mode Falling Edge
	0	0	Window mode
1	0	1	Programmable Divider output
1	1	0	Pulse Width Modulation output
1	1	1	Buzzer (output timer/counter clock source. The duty cycle of the clock source must be 50/50)

Bit 4 (TC1SS0): Timer/Counter 1 clock source select bit

0: Fs is used as counting source (Fc) (default)

1: Fm is used as counting source (Fc)

Bits 3~0 (TC1CK3~TC1CK0): Timer/Counter 1 clock source prescaler select

TC3CK3	TC3CK2	TC3CK1	TC3CK0	Clock Source	Resolution 8 MHz	Max. Time 8 MHz	Resolution 16kHz	Max. Time 16kHz
				Normal	Fc=8M	Fc=8M	Fc=16K	Fc=16K
0	0	0	0	Fc	125ns	32 µs	62.5 µs	16ms
0	0	0	1	Fc/2	250ns	64 µs	125 µs	32ms
0	0	1	0	$Fc/2^2$	500ns	128 µs	250 µs	64ms
0	0	1	1	$Fc/2^3$	1 µs	256 µs	500 µs	128ms
0	1	0	0	$Fc/2^4$	2 µs	512 µs	1ms	256ms
0	1	0	1	$Fc/2^5$	4 µs	1024 µs	2ms	512ms
0	1	1	0	$Fc/2^6$	8 µs	2048 µs	4ms	1024ms
0	1	1	1	$Fc/2^7$	16 µs	4096 µs	8ms	2048ms
1	0	0	0	$Fc/2^8$	32 µs	8192 µs	16ms	4096ms
1	0	0	1	$Fc/2^9$	64 µs	16384 µs	32ms	8192ms
1	0	1	0	$Fc/2^{10}$	128 µs	32768 µs	64ms	16384ms
1	0	1	1	$Fc/2^{11}$	256 µs	65536 µs	128ms	32768ms
1	1	0	0	$Fc/2^{12}$	512 µs	131072 µs	256ms	65536ms
1	1	0	1	$Fc/2^{13}$	1.024ms	262144 µs	512ms	131072ms
1	1	1	0	$Fc/2^{14}$	2.048ms	524.288ms	1.024s	262144ms
1	1	1	1	$Fc/2^{15}$	4.096ms	1.048s	2.048s	524288ms

6.1.29 Bank 0 R26 TC1DA (Timer/Counter 1 Data Buffer A)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC1DA7	TC1DA6	TC1DA5	TC1DA4	TC1DA3	TC1DA2	TC1DA1	TC1DA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (TC1DA7~0): Data Buffer A of 8-bit Timer/Counter 1

6.1.30 Bank 0 R27 TC1DB (Timer/Counter 1 Data Buffer B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC1DB7	TC1DB6	TC1DB5	TC1DB4	TC1DB3	TC1DB2	TC1DB1	TC1DB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (TC1DB7~0): Data Buffer B of 8-bit Timer/Counter 1

NOTE

1. *When Timer/Counter x is used in PWM mode, the duty value stored at register TCxDB must be less than or equal to the period value stored at register TCxDA, i.e., duty ≦ period. Then the PWM waveform is generated. If the duty is greater than the period, the PWM output waveform is kept at a **high** voltage level.*
2. *The period value set by users is extra plus 1 in inner circuit.*
   For example:

When the period value is set as 0x4F, the PWM waveform will actually generate 0x50 period length.

When the period value is set as 0xFF, the PWM waveform will actually generate 0x100 period length.

6.1.31 Bank0 R28~35: Reserved

6.1.32 Bank 0 R36 SPICR (SPI Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CES	SPIE	SRO	SSE	SDOC	SBRS2	SBRS1	SBRS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (CES): Clock Edge Select Bit

0: Data shifts out on a rising edge, and shifts in on a falling edge. Data is on hold during a low-level.

1: Data shifts out on a falling edge, and shift in on a rising edge. Data is on hold during a high-level.

Bit 6 (SPIE): SPI Enable Bit

0: Disable SPI mode

1: Enable SPI mode

Bit 5 (SRO): SPI Read Overflow Bit

0: No overflow

1: A new data is received while the previous data is still being held in the SPIR register. In this situation, the data in the SPIS register will be destroyed. To avoid setting this bit, user is required to read the SPIR register although only transmission is implemented. This can only occur in Slave mode.

Bit 4 (SSE): SPI Shift Enable Bit

0: Reset as soon as shifting is completed, and the next byte is ready to be shifted.

1: Start to shift, and remain on “1” while the current byte is still being transmitted.

Bit 3 (SDOC): SDO Output Status Control Bit

0: After the serial data output, the SDO remains high.

1: After the serial data output, the SDO remains low.

Bits 2~0 (SBRS2~SBRS0): SPI Baud Rate Select Bits

SBRS2	SBRS1	SBRS0	Mode	SPI Baud Rate
0	0	0	Master	Fosc/2
0	0	1	Master	Fosc/4
0	1	0	Master	Fosc/8
0	1	1	Master	Fosc/16
1	0	0	Master	Fosc/32
1	0	1	Master	Fosc/64
1	1	0	Slave	/SS enable
1	1	1	Slave	/SS disable

6.1.33 Bank 0 R37 SPIS (SPI Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DORD	TD1	TD0	−	OD3	OD4	−	RBF
R/W	R/W	R/W	−	R/W	R/W	−	R

Bit 7 (DORD): Data Shift Type Control Bit

0: Shift left (MSB first)

1: Shift right (LSB first)

Bits 6~5 (TD1~TD0): SDO Status Output Delay Times Options. When CPU oscillator source use Fs from 1 CLK delay time.

TD1	TD0	Delay Time
0	0	8 CLK
0	1	16 CLK
1	0	24 CLK
1	1	32 CLK

Bit 4: Not used, set to “0” all the time.

Bit 3 (OD3): Open-drain control bit

0: Open-drain disable for SDO

1: Open-drain enable for SDO

Bit 2 (OD4): Open-drain control bit

0: Open-drain disable for SCK

1: Open-drain enable for SCK

Bit 1: Not used, set to “0” all the time.

Bit 0 (RBF): Read Buffer Full Flag

0: Receiving not completed, and SPIR has not fully exchanged.

1: Receiving completed, and SPIR is fully exchanged.

6.1.34 Bank 0 R38 SPIR (SPI Read Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SRB7	SRB6	SRB5	SRB4	SRB3	SRB2	SRB1	SRB0
R	R	R	R	R	R	R	R

Bits 7~0 (SRB7~SRB0): SPI Read Data Buffer

6.1.35 Bank 0 R39 SPIW (SPI Write Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SWB7	SWB6	SWB5	SWB4	SWB3	SWB2	SWB1	SWB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (SWB7~SWB0): SPI Write Data Buffer

6.1.36 Bank 0 R3A CMPCR1 (Comparator Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CRS	CPOUT	CS1	CS0		CC+S1	CC+S0	SDPWMA
R/W	R	R/W	R/W		R/W	R/W	R/W

Bit 7 (CRS): Select reference source for inverting terminal of Comparator/OP

0: CIN- is connected to pad (default)

1: CIN- is connected to internal reference

Bit 6 (CPOUT): The result of comparator output.

Bits 5~4 (CS1 ~ CS0): Comparator Select bits

CS1	CS0	Function Description
0	0	Comparator and CO are not used.
0	1	Comparator is uesd and comparator output is not connected to pad
1	0	Comparator is uesd and comparator output is connected to pad
1	1	OP

Bit 3: Not used, set to "0" all the time.

Bits 2~1 (CC+S1~CC+S0): Comparator CIN+ channel Select bits.

CC+S1	CC+S0	Channel
0	0	CA+
0	1	CB+
1	0	CC+
1	1	CD+

Bit 0 (SDPWMA): Shut down PMWA

0: Disable (default value)

1: Enable. The TAEN is disabled at the falling edge of comparator1.

NOTE

When using internal reference, users need to wait at least 6us after control bits "CIRLx1~CIRLx0" are set, so as to obtain accurate output results. If not, the output result would be inaccurate. Meanwhile, we also suggest not to set control bits "CxS1~CxS0" as (1:0) or (1:1) to prevent unexpected status.

6.1.37 Bank 0 R3B CMPCR2 (Comparator Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
						CIRL2	SDPWMB
						R/W	R/W

Bits 7~2: Not used, set to "0" all the time.

Bit 1 (CIRL2): The high bit of internal voltage reference.

CIRL2	CIRL1	CIRL0	Voltage reference
0	0	0	AVDD (default)
0	0	1	4.096V
0	1	0	3.072V
0	1	1	2.048V
1	1	1	2.56V
1	1	0	2.56V
1	0	1	2.56V
1	0	0	2.56V

Bit 0 (SDPWMB): Shut down PMWB

0: Disable (default value)

1: Enable. The TBEN is disabled at the falling edge of comparator2.

NOTE

When using internal reference, users need to wait at least 6us after control bits "CIRLx1~CIRLx0" are set, so as to obtain accurate output results. If not, the output results would be inaccurate. Meanwhile, we also suggest not to set control bits "CxS1~CxS0" as (1:0) or (1:1) to prevent unexpected status.

6.1.38 Bank 0 R3C CMPCR3 (Comparator Control Register 3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
					CIRL1	CIRL0	
					R/W	R/W	

Bits 7~3: Not used, set to "0" all the time.

Bits 2~1 (CIRL1~CIRL0): The lower two bits of internal voltage reference.

CIRL12	CIRL11	CIRL10	Voltage reference
0	0	0	AVDD (default)
0	0	1	4.096V
0	1	0	3.072V
0	1	1	2.048V
1	1	1	2.56V
1	1	0	2.56V
1	0	1	2.56V
1	0	0	2.56V

Bits 0: Not used, set to "0" all the time.

NOTE

1. *When using internal voltage reference and the code option word2<7:6> is set to "11", users need to wait for at least 50us the first time to enable and stabilize the internal voltage reference circuit. After that, users only need to wait 6us (the least) whenever switching voltage references.*
2. *When using internal voltage reference and the code option word2<7:6> is set to "10", users only need to wait 6us (the least) to stabilize the internal voltage reference circuit whenever switching voltage references.*

6.1.39 Bank 0 R3E ADCR1 (Analog-to-Digital Converter Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CKR2	CKR1	CKR0	ADRUN	ADP	ADOM	SHS1	SHS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~5 (CKR2~0): Clock Rate Selection of ADC

System Mode	CKR2~0	Operating Clock of ADC ($F_{AD} = 1 / T_{AD}$)	Max. F_{Main} (V_{DD} = 2.5V ~ 3V)	Max. F_{Main} (V_{DD} = 3V ~ 5.5V)
Normal Mode	000	$F_{Main}/16$	8 MHz	16 MHz
	001	$F_{Main}/8$	4 MHz	16 MHz
	010	$F_{Main}/4$	2 MHz	8 MHz
	011	$F_{Main}/2$	1 MHz	4 MHz
	100	$F_{Main}/64$	16 MHz	16 MHz
	101	$F_{Main}/32$	16 MHz	16 MHz
	110	$F_{Main}/1$	500kHz	2 MHz
	111	F_{Sub}	Fs	Fs
Green Mode	xxx	F_{Sub}	Fs	Fs

Bit 4 (ADRUN): ADC Starts to Run

In Single mode:

0: Reset by hardware upon completing of the conversion, this bit cannot be reset by software.

1: A/D conversion starts. This bit can be set by software.

In Continuous mode:

0: ADC is stopped

1: ADC is running unless this bit is reset by software

Bit 3 (ADP): ADC Power

0: ADC is in power-down mode.

1: ADC is operating normally.

Bit 2 (ADOM): ADC Operation Mode Select

0: ADC operates in single mode.

1: ADC operates in continuous mode.

Bits 1~0 (SHS1~0): Sample and Hold Timing Select (Recommend at least 4 μs, T_{AD}**:** Period of ADC Operating Clock**)**

SHS1~0	Sample and Hold Timing
00	2 x T_{AD}
01	4 x T_{AD}
10	8 x T_{AD}
11	12 x T_{AD}

6.1.40 Bank 0 R3F ADCR2 (Analog-to-Digital Converter Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	**VPIS2**	ADIM	ADCMS	VPIS1	VPIS0	VREFP	VREFN
–	**R/W**	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7: Not used, set to "0" all the time.

Bit 5 (ADIM): ADC Interrupt Mode

0: Normal mode. Interrupt occurred after AD conversion is completed.

1: Compare mode. Interrupt occurred when comparison result conforms to the setting of ADCMS bits. Continuous mode is recommended.

Bit 4 (ADCMS): ADC Compare Mode Select.

Compare mode:

0: Interrupt occurs when AD conversion data is equal to or greater than the data in ADCD register (which means when ADD ≥ ADCD, interrupt occurs).

1: Interrupt occurs when AD conversion data is equal to or less than the data in ADCD register (which means when ADD ≤ ADCD, interrupt occurs).

Normal mode: No effect

Bits 6, 3 ~ 2 (VPIS2~0): Internal Positive Reference Voltage Selection.

VPIS2	VPIS1	VPIS0	Reference Voltage
0	0	0	AVDD
0	0	1	4.096 V
0	1	0	3.072 V
0	1	1	2.048 V
1	0	0	2.56 V
1	0	1	2.56 V
1	1	0	2.56 V
1	1	1	2.56 V

Bit 1 (VREFP): Positive Reference Voltage Select

0: Internal positive reference voltage. The actual voltage is set by VPIS1~0 bits.

1: From VREF pin.

Bit 0 (VREFN): Negative Reference Voltage Selection

0: Common ground with internal reference voltage.

1: Common ground with VREF pin.

NOTE

1. *When using the internal voltage reference and the Code Option Word 2<6> (IRCIRS) sets to "1", users need to wait for at least 50 µs the first time to enable and stabilize the voltage reference. Un-stabilized reference makes conversion result inaccurate. After that, users only need to wait 6 µs (the least) whenever switching voltage references.*
2. *When using the internal voltage reference and the Code Option Word 2<6> (IRCIRS) sets to "0", users only need to wait for 6 µs (the least) for the internal voltage reference circuit to stabilize whenever switching voltage references.*

6.1.41 Bank 0 R40 ADISR (Analog-to-Digital Converter Input Channel Select Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	ADIS4	ADIS3	ADIS2	ADIS1	ADIS0
–	–	–	R/W	R/W	R/W	R/W	R/W

Bits 7~5: Not used, set to “0” all the time.

Bits 4~0 (ADIS4~0): ADC input channel select bits

ADIS4~0	Selected Channel	ADIS4~0	Selected Channel
00000	AD0	*10000	1/2 VDD Power Detect
00001	AD1	10001	OP
00010	AD2	10010	N/A
00011	AD3	10011	N/A
00100	AD4	10100	N/A
00101	AD5	10101	N/A
00110	AD6	10110	N/A
00111	AD7	10111	N/A
01000	AD8	11000	N/A
01001	AD9	11001	N/A
01010	AD10	11010	N/A
01011	AD11	11011	N/A
01100	N/A	11100	N/A
01101	N/A	11101	N/A
01110	N/A	11110	N/A
01111	N/A	11111	N/A

* *Used for internal signal source. Users only need to set ADIS4~0=10000.*
These AD input channels are instantly active.

6.1.42 Bank 0 R41 ADER1 (Analog-to-Digital Converter Input Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (ADE7): AD converter enable bit of P65 pin.

0: Disable ADC7, P65 acts as I/O pin

1: Enable ADC7 to act as analog input pin

Bit 6 (ADE6): AD converter enable bit of P64 pin.

0: Disable ADC6, P64 acts as I/O pin

1: Enable ADC6 to act as analog input pin

Bit 5 (ADE5): AD converter enable bit of P62 pin.

0: Disable ADC5, P62 acts as I/O pin

1: Enable ADC5 to act as analog input pin

Bit 4 (ADE4): AD converter enable bit of P61 pin.

0: Disable ADC4, P61 acts as I/O pin

1: Enable ADC4 to act as analog input pin

Bit 3 (ADE3): AD converter enable bit of P60 pin.

0: Disable ADC3, P60 acts as I/O pin

1: Enable ADC3 to act as analog input pin.

Bit 2 (ADE2): AD converter enable bit of P54 pin.

0: Disable ADC2, P54 acts as I/O pin

1: Enable ADC2 to act as analog input pin

Bit 1 (ADE1): AD converter enable bit of P53 pin.

0: Disable ADC1, P53 acts as I/O pin

1: Enable ADC1 to act as analog input pin

Bit 0 (ADE0): AD converter enable bit of P52 pin.

0: Disable ADC0, P52 acts as I/O pin

1: Enable ADC0 to act as analog input pin

6.1.43 Bank 0 R42 ADER2 (Analog-to-Digital Converter Input Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
				ADE11	ADE10	ADE9	ADE8
				R/W	R/W	R/W	R/W

Bit 3 (ADE11): AD converter enable bit of P55 pin.

0: Disable ADC11, P55 acts as I/O pin

1: Enable ADC11 to act as analog input pin

Bit 2 (ADE10): AD converter enable bit of P56 pin.

0: Disable ADC10, P56 acts as I/O pin

1: Enable ADC10 to act as analog input pin

Bit 1 (ADE9): AD converter enable bit of P57 pin.

0: Disable ADC9, P57 acts as I/O pin

1: Enable ADC9 to act as analog input pin

Bit 0 (ADE8): AD converter enable bit of P66 pin.

0: Disable ADC8, P66 acts as I/O pin

1: Enable ADC8 to act as analog input pin

6.1.44 Bank 0 R43 ADDL (Low Byte of Analog-to-Digital Converter Data)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADD7	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0
R	R	R	R	R	R	R	R

Bits 7~0 (ADD7~ ADD0): Low Byte of AD Data Buffer

6.1.45 Bank 0 R44 ADDH (High Byte of Analog-to-Digital Converter Data)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADD15	ADD14	ADD13	ADD12	ADD11	ADD10	ADD9	ADD8
R	R	R	R	R	R	R	R

Bits 7~0 (ADD15~ ADD8): High Byte of AD Data Buffer.

The format of AD data is dependent on Code Option ADFM. The following table shows how the data justify the different ADFM settings.

ADFM1~0			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
12 bits	0	ADDH	-	-	-	-	ADD11	ADD10	ADD9	ADD8
		ADDL	ADD7	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0
	1	ADDH	ADD11	ADD10	ADD9	ADD8	ADD7	ADD6	ADD5	ADD4
		ADDL	-	-	-	-	ADD3	ADD2	ADD1	ADD0

6.1.46 Bank 0 R45 ADCVL (Low Byte of Analog-to-Digital Converter Compare Value)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADCD7	ADCD6	ADCD5	ADCD4	ADCD3	ADCD2	ADCD1	ADCD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (ADCD7~0): Low Byte Data for AD Comparison.

User should use the data format as with ADDH and ADDL registers. Otherwise, incorrect values will yield after AD comparison.

6.1.47 Bank 0 R46 ADCVH (High Byte of Analog-to-Digital Converter Compare Value)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADCD15	ADCD14	ADCD13	ADCD12	ADCD11	ADCD10	ADCD9	ADCD8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (ADCD15~8): High Byte Data for AD Comparison

User should use the data format as with ADDH and ADDL registers. Otherwise, incorrect values will yield aft er AD comparison.

6.1.48 Bank 1 R5 IOCR8

These registers are used to control I/O port direction. They are both readable and writable.

0: Put the relative I/O pin as output

1: Put the relative I/O pin into high impedance

6.1.49 Bank 1 R8 P5PHCR (Port 5 Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PH57	PH56	PH55	PH54	PH53	PH52	PH51	PH50
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (PH57~PH50): Control bits used to enable pull-high of P57~P50 pins

0: Enable internal pull-high

1: Disable internal pull-high

6.1.50 Bank 1 R9 P6PHCR (Port 6 Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PH67	PH66	PH65	PH64	PH63	PH62	PH61	PH60
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (PH67~PH60): Control bits used to enable pull-high of P67~P60 pins

0: Enable internal pull-high

1: Disable internal pull-high

6.1.51 Bank 1 RA P8PHCR (Port 7~8 Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
					P8LPH		
					R/W		

Bits 7~3: Not used, set to "0" all the time.

Bit 2 (P8LPH): Control bit used to enable pull-high of Port8 low nibble pin

1: Disable internal pull-high (default)

0: Enable internal pull-high

Bits 1~0: Not used, set to "0" all the time.

6.1.52 Bank 1 RB P5PLCR (Port 5 Pull-low Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PL57	PL56	PL55	PL54	PL53	PL52	PL51	PL50
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (PL57~PL50): Control bits used to enable pull-low of P57~P50 pins

0: Enable internal pull-low

1: Disable internal pull-low

6.1.53 Bank 1 RC P6PLCR (Port 6 Pull-low Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PL67	PL66	PL65	PL64	PL63	PL62	PL61	PL60
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (PL67~PL60): Control bits used to enable pull-low of P67~P60 pins

0: Enable internal pull-low

1: Disable internal pull-low

6.1.54 Bank 1 RD P8PLCR (Port 8 Pull-low Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
					P8LPL		
					R/W		

Bits 7~3: Not used, set to "0" all the time.

Bit 2 (P8LPL): Control bit used to enable pull-low of Port 8 low nibble pin

1: Disable internal pull-low (default)

0: Enable internal pull-low

Bits 1~0: Not used, set to "0" all the time.

6.1.55 Bank 1 RE P5HDSCR (Port 5 High Drive/Sink Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
H57	H56	H55	H54	H53	H52	H51	H50
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (H57~H50): P57~P50 high drive/sink current control bits

0: Enable high drive/sink

1: Disable high drive/sink

6.1.56 Bank 1 RF P6HDSCR (Port 6 High Drive/Sink Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
H67	H66	H65	H64	H63	H62	H61	H60
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (H67~H60): P67~P60 high drive/sink current control bits

0: Enable high drive/sink

1: Disable high drive/sink

6.1.57 Bank 1 R10 P8HDSCR (Port 8 High Drive/Sink Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
					P8LHDS		
					R/W		

Bits 7~3: Not used, set to "0" all the time.

Bit 2 (P8LHDS): Control bit used to enable high drive/sink of Port 8 low nibble pin

1: Disable high drive/sink (default)

0: Enable high drive/sink

Bits 1~0: Not used, set to "0" all the time.

6.1.58 Bank 1 R11 P5ODCR (Port 5 Open-drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OD57	OD56	OD55	OD54	OD53	OD52	OD51	OD50
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (OD57~OD50): P57~P50 Open-drain control bits

0: Disable open-drain function

1: Enable open-drain function

6.1.59 Bank 1 R12 P6ODCR (Port 6 Open-drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OD67	OD66	OD65	OD64	OD63	OD62	OD61	OD60
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (OD67~OD60): P67~P60 Open-drain control bits

0: Disable open-drain function

1: Enable open-drain function

6.1.60 Bank 1 R13 P8ODCR (Ports 8 Open-drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
					P8LOD		
					R/W		

Bits 7~3: Not used, set to "0" all the time

Bit 2 (P8LOD): Control bit used to enable open-drain of Port 8 low nibble pin

0: Disable open-drain function (default)

1: Enable open-drain function

Bits 1~0: Not used, set to "0" all the time.

6.1.61 Bank 1 R14 DeadTCR (Dead Time Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
				DEADTBE	DEADTAE	DEADTP1	DEADTP0
				R/W	R/W	R/W	R/W

Bits 7~4: Not used, set to "0" all the time

Bit 3 (DEADTBE): Enable dead-time function for PWMB and /PWMB (for dual PWM)

0: Disable (default)

1: Enable.

Bit 2 (DEADTAE): Enable dead-time function for PWMA and /PWMA (for dual PWM)

0: Disable (default)

1: Enable.

Bits 1~0 (DEADTP1~DEADTP0): Dead-time prescaler

DEADTP1	DEADTP0	Prescale
0	0	1:1 (default)
0	1	1:2
1	0	1:4
1	1	1:8

NOTE

The dead-time function is used only for dual PWM. When using single PWM function (not dual PWM), the dead-time function is always disabled.

6.1.62 Bank 1 R15 DeadTR (Dead Time Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
				DEADTR3	DEADTR2	DEADTR1	DEADTR0
				R/W	R/W	R/W	R/W

Bits 7~4 (DEADTR7~4): Not used, set to "0" all the time

Bits 3~0 (DEADTR3~0): The contents of the register are dead-time

6.1.63 Bank 1 R16 PWMSCR (PWM Source Clock Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
			DEADS			PWMBS	PWMAS
			R/W			R/W	R/W

Bits 7~5: Not used, set to "0" all the time.

Bit 4 (DEADS): Clock selection for dead-time timer

0: Fs (default)

1: Fm

Bit 3~2: Not used, set to "0" all the time.

Bit 1 (PWMBS): Clock selection for PWMB timer

0: Fs (default)

1: Fm

Bit 0 (PWMAS): Clock selection for PWMA timer

0: Fs (default)

1: Fm

6.1.64 Bank 1 R17 PWMACR (PWMA Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWMAE	IPWMAE	PWMAA	IPWMAA	TAEN	TAP2	TAP1	TAP0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (PWMAE): PWMA enable bit

0: Disable (default)

1: Enable. The compound pin is used as PWMA pin

Bit 6 (IPWMAE): Inverse PWMA enable bit

0: Disable (default)

1: Enable. The compound pin is used as /PWMA pin

Bit 5 (PWMAA): Active level of PWMA

0: Duty-deadtime is logic 1 (default)

1: Duty-deadtime is logic 0

Bit 4 (IPWMAA): active level of inverse PWMA

0: Period-duty-deadtime is logic 1 (default)

1: Period-duty-deadtime is logic 0

Bit 3 (TAEN): TMRA enable bit. All PWM function are valid only as this bit is set

0: TMRA is off (default value)

1: TMRA is on

PWMXEN	TXEN	Function description
0	0	Not used as PWM function; I/O pin or other functional pins.
0	1	Timer function; I/O pin or other function pins.
1	0	PWM function, the waveform remains at inactive level.
1	1	PWM function, the normal PWM output waveform.

Bits 2~0 (TAP2~TAP0): TMRA clock prescale option bits

TAP2	TAP1	TAP0	Prescale
0	0	0	1:1 (default)
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.1.65 Bank 1 R18 PRDAL (Low byte of PWMA period)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRDA7	PRDA6	PRDA5	PRDA4	PRDA3	PRDA2	PRDA1	PRDA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (PRDA7~0): The contents of the register are low byte of the PWMA period.

6.1.66 Bank 1 R19 PRDAH (High byte of PWMA period)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
						PRDA9	PRDA8
						R/W	R/W

Bits 7~2: Not used, set to "0" all the time.

Bits 1~0 (PRDA9~8): The contents of the register are high byte of PWMA period.

6.1.67 Bank 1 R1A DTAL (Low byte of PMWA duty)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DTA7	DTA6	DTA5	DTA4	DTA3	DTA2	DTA1	DTA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (DTA7~0): The contents of the register are low byte of the PWMA duty.

6.1.68 Bank 1 R1B DTAH (High byte of PMWA duty)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
						DTA9	DTA8
						R/W	R/W

Bits 7~2: Not used, set to "0" all the time.

Bits 1~0 (DTA9~8): The contents of the register are high byte of the PWMA duty.

6.1.69 Bank 1 R1C TMRAL (Low byte of TimerA)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMRA7	TMRA6	TMRA5	TMRA4	TMRA3	TMRA2	TMRA1	TMRA0
R	R	R	R	R	R	R	R

Bits 7~0 (TMRA7~0): The contents of the register are low byte of the PWMA timer which is counting. This is read-only.

6.1.70 Bank 1 R1D TMRAH (High byte of TimerA)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
						TMRA9	TMRA8
						R	R

Bits 7~2: Not used, set to "0" all the time.

Bits 1~0 (TMRA9~8): The contents of the register are high byte of the PWMA timer which is counting. This is read-only.

6.1.71 Bank 1 R1E PWMBCR (PWMB Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWMBE	IPWMBE	PWMBA	IPWMBA	TBEN	TBP2	TBP1	TBP0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (PWMBE): PWMB enable bit

0: Disable (default)

1: Enable. The compound pin is used as PWMB pin

Bit 6 (IPWMBE): Inverse PWMB enable bit

0: Disable (default)

1: Enable. The compound pin is used as /PWMB pin

Bit 5 (PWMBA): Active level of PWMB

0: duty-deadtime is logic 1 (default)

1: duty-deadtime is logic 0

Bit 4 (IPWMBA): Active level of inverse PWMB

0: period-duty-deadtime is logic 1 (default)

1: period-duty-deadtime is logic 0

Bit 3 (TBEN): TMRB enable bit. All PWM functions are valid only as this bit is set

0: TMRB is off (default value)

1: TMRB is on

Bits 2~0 (TBP2~TBP0): TMRB clock prescale option bits

TBP2	TBP1	TBP0	Prescale
0	0	0	1:1 (default)
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.1.72 Bank 1 R1F PRDBL (Low byte of PWMB period)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRDB7	PRDB6	PRDB5	PRDB4	PRDB3	PRDB2	PRDB1	PRDB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (PRDB7~0): The contents of the register are low byte of the PWMB period

6.1.73 Bank 1 R20 PRDBH (High byte of PWMB period)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
						PRDB9	PRDB8
						R/W	R/W

Bits 7~2: Not used, set to "0" all the time.

Bits 1~0 (PRDB9~8): The contents of the register are high byte of PWMB period

6.1.74 Bank 1 R21 DTBL (Low byte of PMWB duty)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DTB7	DTB6	DTB5	DTB4	DTB3	DTB2	DTB1	DTB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (DTB7~0): The contents of the register are low byte of the PWMB duty

6.1.75 Bank 1 R22 DTBH (High byte of PMWB duty)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
						DTB9	DTB8
						R/W	R/W

Bits 7~2: Not used, set to "0" all the time.

Bits 1~0 (DTB9~8): The contents of the register are high byte of the PWMB duty

6.1.76 Bank 1 R23 TMRBL (Low byte of TimerB)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMRB7	TMRB6	TMRB5	TMRB4	TMRB3	TMRB2	TMRB1	TMRB0
R	R	R	R	R	R	R	R

Bits 7~0 (TMRB7~0): The contents of the register are low byte of the PWMB timer which is counting. This is read-only.

6.1.77 Bank 1 R24 TMRBH (High byte of TimerB)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
						TMRB9	TMRB8
						R	R

Bits 7~2: Not used, set to "0" all the time.

Bits 1~0 (TMRB9~8): The contents of the register are high byte of the PWMB timer which is counting. This is read-only.

6.1.78 Bank1 R25 ~ R32: (Reserved)

6.1.79 Bank 1 R33 URCR (UART Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
UINVEN	UMODE1	UMODE0	BRATE2	BRATE1	BRATE0	UTBE	TXE
R/W	R/W	R/W	R/W	R/W	R/W	R	R/W

Bit 7 (UINVEN): Enable UART TXD and RXD Port Inverse Output Bit

0: Disable TXD and RXD port inverse output

1: Enable TXD and RXD port inverse output

Bits 6~5 (UMODE1~UMODE0): UART mode select bits

UMODE1	UMODE0	UART Mode
0	0	7-bit
0	1	8-bit
1	0	9-bit
1	1	Reserved

Bits 4~2 (BRATE2~BRATE0): Transmit Baud rate select (T_{UART}=Fc/16)

BRATE2	BRATE1	BRATE0	Baud Rate	8 MHz
0	0	0	T_{UART}/13	38400
0	0	1	T_{UART}/26	19200
0	1	0	T_{UART}/52	9600
0	1	1	T_{UART}/104	4800
1	0	0	T_{UART}/208	2400
1	0	1	T_{UART}/416	1200
1	1	0	Reserved	
1	1	1	Reserved	

Bit 1 (UTBE): UART transfer buffer empty flag. Set to "1" when transfer buffer is empty. Reset to "**0**" automatically when writing to the URTD register. The UTBE bit will be cleared by hardware when enabling transmission. The UTBE bit is read-only. Therefore, writing to the URTD register is necessary in starting transmission shifting.

Bit 0 (TXE): Enable transmission

0: Disable

1: Enable

6.1.80 Bank 1 R34 URS (UART Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URTD8	EVEN	PRE	PRERR	OVERR	FMERR	URBF	RXE
W	R/W	R/W	R/W	R/W	R/W	R	R/W

Bit 7 (URTD8): UART Transmit Data Bit 8. Write-only.

Bit 6 (EVEN): Select parity check

0: Odd parity

1: Even parity

Bit 5 (PRE): Enable parity addition

0: Disable

1: Enable

Bit 4 (PRERR): Parity error flag. Set to 1 when parity error occurred, cleared to 0 by software.

Bit 3 (OVERR): Over running error flag. Set to 1 when overrun error occurred, cleared to 0 by software.

Bit 2 (FMERR): Framing error flag. Set to 1 when framing error occurred, cleared to 0 by software.

Bit 1 (URBF): UART read buffer full flag. Set to 1 when one character is received. Reset to 0 automatically when read from the URS register. URBF will be cleared by hardware when enabling receiving. The URBF bit is read-only. Therefore, reading the URS register is necessary to avoid overrun error.

Bit 0 (RXE): Enable receiving

0: Disable

1: Enable

6.1.81 Bank 1 R35 URTD (UART Transmit Data Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URTD7	URTD6	URTD5	URTD4	URTD3	URTD2	URTD1	URTD0
W	W	W	W	W	W	W	W

Bits 7~0 (URTD7~URTD0): UART transmit data buffer. Write-only.

6.1.82 Bank 1 R36 URRDL (UART Receive Data Low Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URRD7	URRD6	URRD5	URRD4	URRD3	URRD2	URRD1	URRD0
R	R	R	R	R	R	R	R

Bits 7~0 (URRD7~URRD0): UART Receive Data Buffer. **Read-only**.

6.1.83 Bank 1 R37 URRDH (UART Receive Data High Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URRD8	–	–	–	–	–	–	URSS
R	–	–	–	–	–	–	R/W

Bit 7 (URRD8): UART Receive Data Bit 8. **Read-only.**

Bits 6~1: Not used, set to “0” all the time.

Bit 0 (URSS): UART clock source select bit.

0: Fc is set to Fs

1: Fc is set to Fm

6.1.84 Bank 1 R45 TBPTL (Table Pointer Low Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TB7	TB6	TB5	TB4	TB3	TB2	TB1	TB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (TB7~TB0): Table Pointer Address Bits 7~0.

6.1.85 Bank 1 R46 TBPTH (Table Pointer High Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HLB	GP	GP	GP	TB11	TB10	TB9	TB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (HLB): Take High Byte or Low Byte content of Flash ROM addressed by TPBTH and TPBTL.

HLB	Read to Register Data Value Description
0	Read Low Byte
1	Read High Byte

Bits 6~4 (GP): General Purpose read/write bits.

Bits 3~0 (TB11~TB8): Table Pointer Address Bits 11~8.

6.1.86 Bank 1 R47 STKMON (Stack Monitor)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STOV	–	–	–	–	STL2	STL1	STL0
R	–	–	–	–	R	R	R

Bit 7 (STOV): Stack pointer overflow indication bit. Read-only.

Bits 6~3: Not used, set to "0" all the time.

Bits 2~0 (STL3~ STL0): Stack pointer number. Read-only.

6.1.87 Bank 1 R48 PCH (Program Counter High)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	–	PC11	PC10	PC9	PC8
–	–	–	–	R/W	R/W	R/W	R/W

Bits 7~4: Not used, set to "0" all the time.

Bits 3~0 (PC11~PC8): Program Counter high byte.

6.1.88 Bank 1 R49 HLVDCR (High/Low Voltage Detector Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HLVDEN	IRVSF	VDSB	VDM	HLVDS3	HLVDS2	HLVDS1	HLVDS0
R/W	R	R	R/W	R/W	R/W	R/W	R/W

Bit 7 (HLVDEN): High/Low Voltage Detector Enable Bit

0: Disable low voltage detector

1: Enable low voltage detector

Bit 6 (IRVSF): Internal Reference Voltage Stable Flag bit

1: Indicate that the voltage detect logic will generate the interrupt flag at the specified voltage range

0: Indicate that the voltage detect logic will not generate the interrupt flag at the specified voltage range and the HLVD interrupt should not be enabled

Bit 5 (VDSB): Voltage Detector State Bit. This is a read-only bit.

1: VDD > HLVD trip point (HLVDS<3:0>)

0: VDD < HLVD trip point (HLVDS<3:0>)

Bit 4 (VDM): Voltage Direction Magnitude Select bit

1: Event occurs when voltage equals or exceeds trip point (HLVDS<3:0>)

0: Event occurs when voltage equals or falls below trip point (HLVDS<3:0>)

HLVDIE	HLVDEN	VDM	IRVSF	VDSB	HLVDSF	Interrupt
0	1	1	1	0->1	0->1	Not happened
0	1	1	1	1->0	0	Not happened
0	1	0	1	0->1	0	Not happened
0	1	0	1	1->0	0->1	Not happened
1	0	X	X	1	0	Not happened
1	1	X	0	X	0	Not happened
1	1	1	1	0->1	0->1	Happened
1	1	1	1	1->0	0	Not happened
1	1	0	1	0->1	0	Not happened
1	1	0	1	1->0	0->1	Happened

Bits 3~0 (HLVDS3~HLVDS0): High/Low Voltage Detector Level Bits

HLVDS3	HLVDS2	HLVDS1	HLVDS0	HLVD Voltage Level
0	0	0	0	4.7V
0	0	0	1	4.5V
0	0	1	0	4.3V
0	0	1	1	4.1V
0	1	0	0	3.9V
0	1	0	1	3.7V
0	1	1	0	3.5V
0	1	1	1	3.3V
1	0	0	0	3.1V
1	0	0	1	2.9V
1	0	1	0	2.8V
1	0	1	1	2.6V
1	1	0	0	2.5V
1	1	0	1	2.4V
1	1	1	0	2.3V
1	1	1	1	2.2V

6.1.89 Bank 1 R4A~R4C: (Reserve)

6.1.90 R50~R7F, Bank 0 R80~RFF

All of these are 8-bit general-purpose registers.

6.2 WDT and Prescaler

There are two 8-bit counters available as prescalers for the WDT. The WPSR0~WPSR2 bits of the WDTCR register (Bank 0 R21) are used to determine the prescaler of WDT. The WDT and prescaler counter will be cleared by the "WDTC" and "SLEP" instructions. Figure 6-3 depicts the Block Diagram of WDT.

The Watchdog timer is a free running on-chip RC oscillator. The WDT will keep on running even after the oscillator driver has been turned off (i.e., in sleep mode). During normal operation or sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled at any time during normal mode by software programming. Refer to WDTE bit of WDTCR (Bank 0 R21) register. With no prescaler, the WDT time-out period is approximately 16 ms(one oscillator start-up timer period).

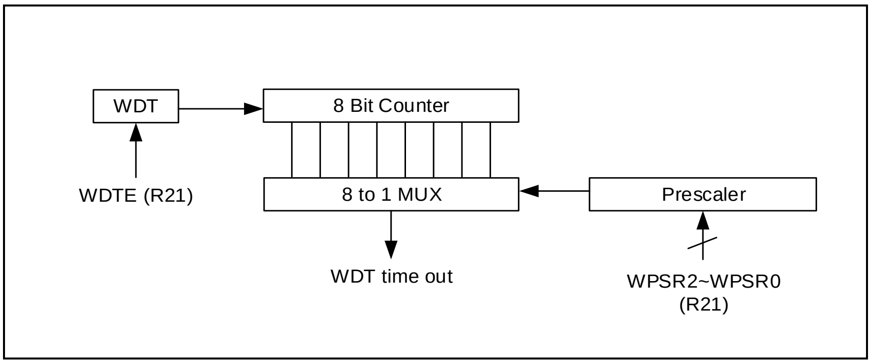
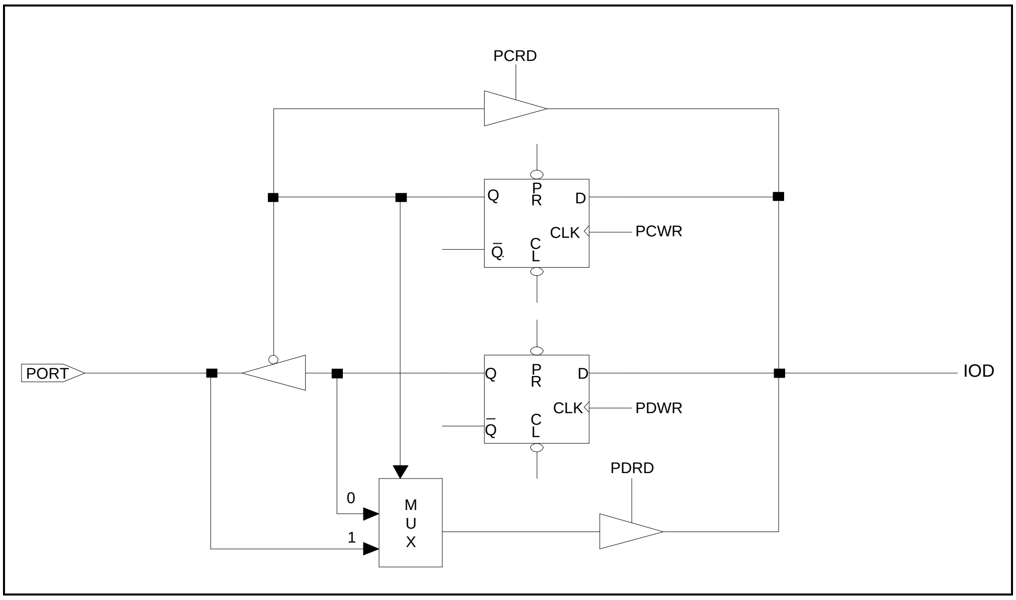


Figure 6-3 WDT Block Diagram

6.3 I/O Ports

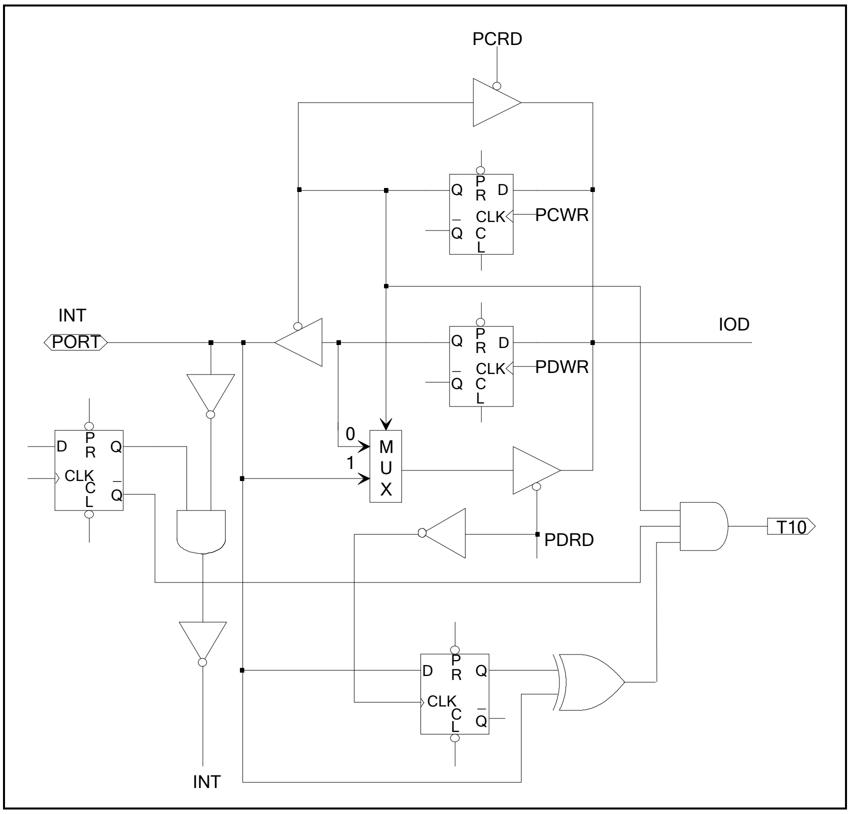
The I/O registers, Port 5~Port 8 are bidirectional tri-state I/O ports. All can be pulled-high and pulled-low internally by software. In addition, they can also have open-drain output and high sink/drive setting by software. Also, Ports 5~8 have wake up and interrupt function. Furthermore, Ports 5~8 also have input status change interrupt functions. Each I/O pin can be defined as an "input" or "output" pin by the I/O control registers (IOC5 ~ IOC8).

The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits for Port 5 ~ Port 8 are shown in Figures 6-4 ~ 6-7.



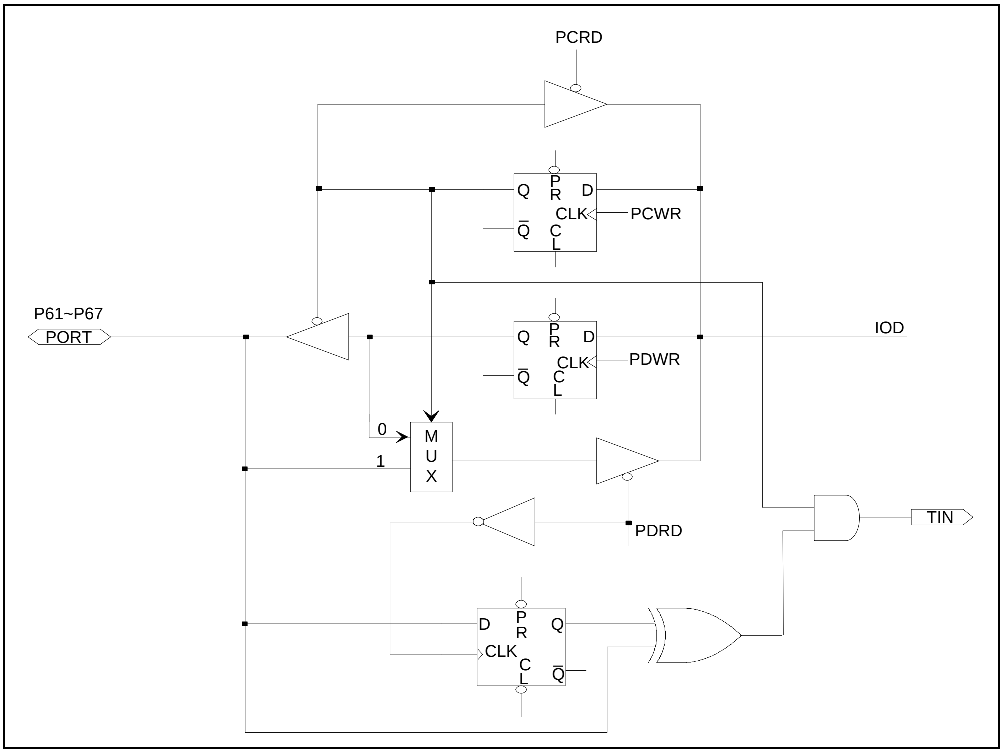
Note: Pull-down is not shown in the figure.

Figure 6-4 Circuit of I/O Port and I/O Control Register for Port 5~8



Note: Pull-high (down) and Open-drain are not shown in the figure.

Figure 6-5 Circuit of I/O Port and I/O Control Register for /INT



Note: Pull-high (down) and Open-drain are not shown in the figure.

Figure 6-6 Circuit of I/O Port and I/O Control Register for Ports 5~8

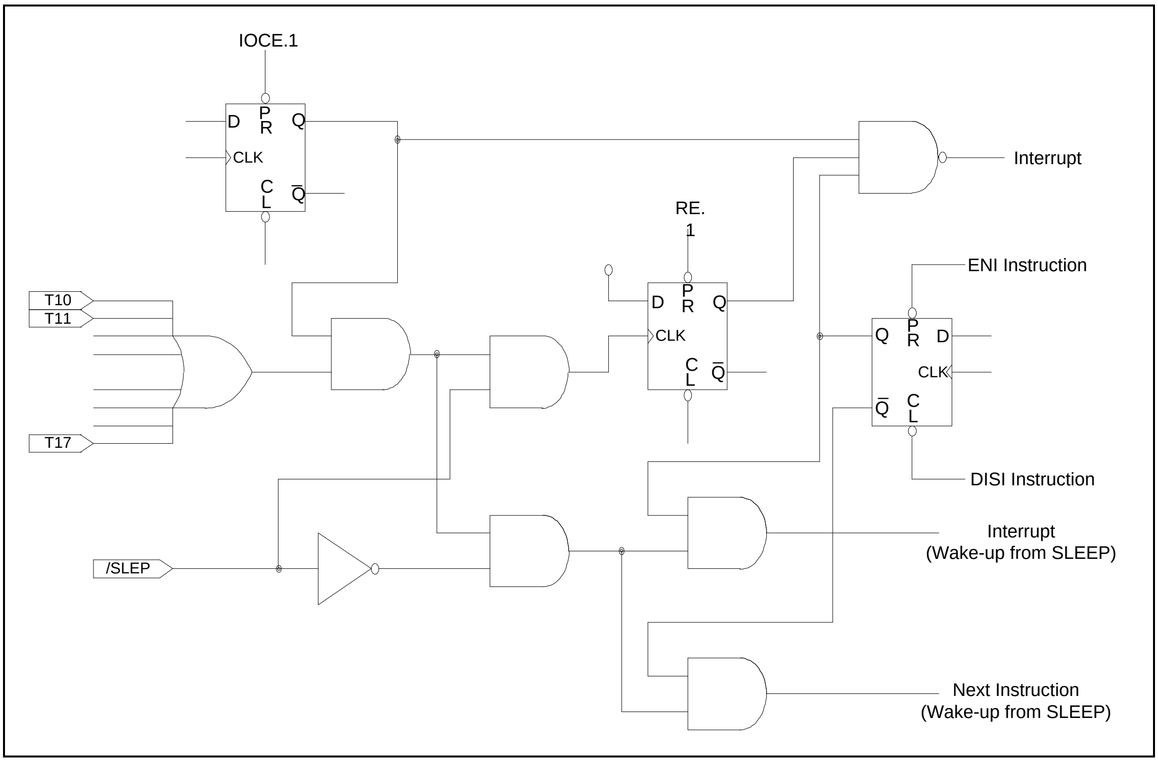


Figure 6-7 Block Diagram of I/O Port 5~8 with Input Change Interrupt/Wake-up

Table 1 Usage of Ports 5~8 Input Changed Wake-up/Interrupt Function

Usage of Ports 5~8 Input Status Changed Wake-up/Interrupt	
(I) Wake-up	(II) Wake-up and interrupt
(a) Before Sleep	(a) Before Sleep
1. Disable WDT	1. Disable WDT
2. Read I/O Port (MOV R6,R6)	2. Read I/O Port (MOV R6, R6)
3. Execute "ENI" or "DISI"	3. Execute "ENI" or "DISI"
4. Enable wake-up bit (Set WUE6H=1, WUE6L=1)	4. Enable wake-up bit (Set WUE6H=1, WUE6L=1)
5. Execute "SLEP" instruction	5. Enable interrupt (Set ICIE =1)
(b) After wake-up	6. Execute "SLEP" instruction
→ Next instruction	(b) After wake-up
	1. IF "ENI" → Interrupt vector (0006H)
	2. IF "DISI" → Next instruction

6.4 Reset and Wake-up

6.4.1 Reset

A reset is initiated by one of the following events:

(1) Power-on reset

(2) /RESET pin input "low"

(3) WDT time-out (if enabled)

(4) LVR (if enabled)

The device is kept in a reset condition for a period of approximately 16ms(one oscillator start-up timer period) after the reset is detected. If the /Reset pin goes “low” or WDT time-out is active, a reset is generated. In IRC mode, the reset time is WSTO and 8 clocks; in High XTAL mode, the reset time is WSTO and 510 clocks; and in low XTAL mode, the reset time is WSTO and 510 clocks (Fsub). Once a reset occurs, the following functions are performed. Refer to Figure 6-8.

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "0".
- All I/O port pins are configured as input mode (high-impedance state).
- The Watchdog timer and prescaler are cleared.
- The control register bits are set according to the entries shown in Table 2 *Summary of Register Initial Values after Reset.*

Sleep (power down) mode is asserted by executing the “SLEP” instruction. While entering sleep mode, WDT (if enabled) is cleared but keeps on running. After wake-up is generated, the wake-up time in IRC mode is WSTO and 8 clocks, WSTO and 510 clocks in High XTAL mode, and WSTO and 510 clocks (Fsub) in low XTAL mode. The controller can be awakened by:

(1) External reset input on /RESET pin.

(2) WDT time-out (if enabled).

(3) External (/INT) pin changes (if INTWKX is enabled).

(4) Port input status changes (if ICWKPX is enabled).

(5) SPI received data when SPI acts as a Slave device (if SPIWK is enabled).

(6) High / Low Voltage Detector (if HLVDWK enable).

(7) A/D conversion completed (if ADWK is enabled).

(8) Comparator output status change (if CMPWK is enabled).

The first two cases will cause the EM88F712N to reset. The T and P flags of R3 can be used to determine the source of the reset (wake-up). Case 3~8 are considered the continuation of program execution and the global interrupt ("ENI" or "DISI" being executed) determines whether or not the controller branches to the interrupt vector following a wake-up. If ENI is executed before SLEP, the instruction will begin to execute from the Address 0X02~0X38 by each interrupt vector after wake-up. If DISI is executed before SLEP, the execution will restart from the instruction right next to SLEP after wake-up.

Only one of Cases 3~8 can be enabled before entering into sleep mode. That is,

[a] If WDT is enabled before SLEP, the EM88F712N can be woken-up only by Case 1 or Case 2. For further details, refer to Section 6.5 *Interrupt*.

[b] If the External (INT9~0) pin change is used to wake up the EM88F712N and the INTWKX bit is enabled before SLEP, WDT must be disabled. Hence, the EM88F712N can be woken up only by Case 3.

[c] If Port Input Status Change is used to wake-up the EM88F712N and the corresponding wake-up setting is enabled before SLEP, WDT must be disabled. Hence, the EM88F712N can be woken up only by Case 4.

[d] When SPI acts as Slave device, after receiving data the EM88F712N will wake-up and the SPIWK bit of Bank 0 R11 register is enabled before SLEP, WDT must be disabled by software. Hence, the EM88F712N can be woken up only by Case 5.

[e] If High/Low voltage detector is used to wake-up the EM88F712N and the HLVDWK bit of Bank 0 R10 register is enabled before SLEP, WDT must be disabled by software. Hence, the EM88F712N can be woken up only by Case 7.

[f] If AD conversion completed is used to wake up the EM88F712N and the ADWK bit of Bank 0 R10 register is enabled before SLEP, WDT must be disabled by software. Hence, the EM88F712N can be woken up only by Case 8.

[g] If Comparator output status change is used to wake up EM88F712N and CMPWK bits of Bank0 R10 & R11 registers is enabled before SLEP, WDT must be disabled by software. Hence, the EM88F712N can be woken up only by Case 9

Table 2 All kinds of Wake-up modes and Interrupt modes are shown below:

<table>
<tr><th rowspan="2">Wake-up Signal</th><th rowspan="2">Condition Signal</th><th colspan="2">Sleep Mode</th><th colspan="2">Idle Mode</th><th colspan="2">Green Mode</th><th colspan="2">Normal Mode</th></tr>
<tr><th>DISI</th><th>ENI</th><th>DISI</th><th>ENI</th><th>DISI</th><th>ENI</th><th>DISI</th><th>ENI</th></tr>
<tr><td rowspan="2">PWMA/B (When timerA/B match PRDA/B)</td><td>PWMxPIE = 0</td><td rowspan="2" colspan="2">Wake-up is invalid</td><td colspan="2">Wake-up is invalid</td><td colspan="2">Interrupt is invalid</td><td colspan="2">Interrupt is invalid</td></tr>
<tr><td>PWMxPIE = 1</td><td>Wake up + Next Instruction</td><td>Wake up + Interrupt Vector</td><td>Next Instruction</td><td>Interrupt + Interrupt Vector</td><td>Next Instruction</td><td>Interrupt + Interrupt Vector</td></tr>
<tr><td rowspan="2">PWMA/B (When timerA/B match DTA/B)</td><td>PWMxDIE = 0</td><td rowspan="2" colspan="2">Wake-up is invalid</td><td colspan="2">Wake-up is invalid</td><td colspan="2">Interrupt is invalid</td><td colspan="2">Interrupt is invalid</td></tr>
<tr><td>PWMxDIE = 1</td><td>Wake up + Next Instruction</td><td>Wake up + Interrupt Vector</td><td>Next Instruction</td><td>Interrupt + Interrupt Vector</td><td>Next Instruction</td><td>Interrupt + Interrupt Vector</td></tr>
<tr><td rowspan="2">TC1/2/3 Interrupt (Used as Timer)</td><td>TC1/2/3IE=0</td><td rowspan="2" colspan="2">Wake-up is invalid</td><td colspan="2">Wake-up is invalid</td><td colspan="2">Interrupt is invalid</td><td colspan="2">Interrupt is invalid</td></tr>
<tr><td>TC1/2/3IE=1</td><td>Wake up + Next Instruction</td><td>Wake up + Interrupt Vector</td><td>Next Instruction</td><td>Interrupt + Interrupt Vector</td><td>Next Instruction</td><td>Interrupt + Interrupt Vector</td></tr>
<tr><td rowspan="2">TC1/2/3 Interrupt (Used as Counter)</td><td>TC1/2/3IE=0</td><td colspan="2">Wake-up is invalid</td><td colspan="2">Wake-up is invalid</td><td colspan="2">Interrupt is invalid</td><td colspan="2">Interrupt is invalid</td></tr>
<tr><td>TC1/2/3IE=1</td><td>Wake up + Next Instruction</td><td>Wake up + Interrupt Vector</td><td>Wake up + Next Instruction</td><td>Wake up + Interrupt Vector</td><td>Next Instruction</td><td>Interrupt + Interrupt Vector</td><td>Next Instruction</td><td>Interrupt + Interrupt Vector</td></tr>
<tr><td rowspan="2">Watch Timer</td><td>WTIE=0</td><td rowspan="2" colspan="2">Wake-up is invalid</td><td colspan="2">Wake-up is invalid.</td><td colspan="2">Interrupt is invalid.</td><td colspan="2">Interrupt is invalid.</td></tr>
<tr><td>WTIE=1</td><td>–</td><td>Wake up + Interrupt Vector</td><td>Next Instruction</td><td>Interrupt + Interrupt Vector</td><td>Next Instruction</td><td>Interrupt + Interrupt Vector</td></tr>
</table>

(Continuation)

Wake-up Signal	Condition Signal	Sleep Mode DISI	Sleep Mode ENI	Idle Mode DISI	Idle Mode ENI	Green Mode DISI	Green Mode ENI	Normal Mode DISI	Normal Mode ENI
External INT	INTWKx = 0, EXIEx = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	INTWKx = 0, EXIEx = 1	Wake-up is invalid		Wake-up is invalid		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	INTWKx = 1, EXIEx = 0	Wake up + Next Instruction		Wake up + Next Instruction		Interrupt is invalid		Interrupt is invalid	
	INTWKx = 1, EXIEx = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
Pin change	ICWKPx = 0, PxICIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	ICWKPx = 0, PxICIE = 1	Wake-up is invalid		Wake-up is invalid		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	ICWKPx = 1, PxICIE = 0	Wake up + Next Instruction		Wake up + Next Instruction		Interrupt is invalid		Interrupt is invalid	
	ICWKPx = 1, PxICIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
Comparator (Comparator output status change)	CMPWK=0 CMPIE=0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	CMPWK=0 CMPIE=1	Wake-up is invalid		Wake-up is invalid		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	CMPWK=1 CMPIE=0	Wake up + Next Instruction		Wake up + Next Instruction		Interrupt is invalid		Interrupt is invalid	
	CMPWK=1 CMPIE=1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
AD Conversion complete	ADWK = 0, ADIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	ADWK = 0, ADIE = 1	Wake-up is invalid		Wake-up is invalid		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	ADWK = 1, ADIE = 0	Wake up + Next Instruction		Wake up + Next Instruction		Interrupt is invalid		Interrupt is invalid	
	ADWK = 1, ADIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
SPI (Slave mode)	SPIWK = 0, SPIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	SPIWK = 0, SPIE = 1	Wake-up is invalid		Wake-up is invalid		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	SPIWK = 1, SPIE = 0	Wake up + Next Instruction		Wake up + Next Instruction		Interrupt is invalid		Interrupt is invalid	
	SPIWK = 1, SPIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector

(Continuation)

Wake-up Signal	Condition Signal	Sleep Mode		Idle Mode		Green Mode		Normal Mode	
		DISI	ENI	DISI	ENI	DISI	ENI	DISI	ENI
UART Transmit complete Interrupt	UTIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid.		Interrupt is invalid.	
	UTIE = 1					Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
UART Receive data Buffer full Interrupt	URIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	URIE = 1					Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
UART Receive Error Interrupt	UERRIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	UERRIE = 1					Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
High / Low Voltage Detector	HLVDWK = 0, HLVDIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	HLVDWK = 0, HLVDIE = 1	Wake-up is invalid		Wake-up is invalid		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	HLVDWK = 1, HLVDIE = 0	Wake up + Next Instruction		Wake up + Next Instruction		Interrupt is invalid		Interrupt is invalid	
	HLVDWK = 1, HLVDIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
Low Voltage Reset		Wake up + Reset		Wake up + Reset		Reset		Reset	
WDT Timeout		Wake up + Reset		Wake up + Reset		Reset		Reset	

6.4.2 *Status of RST, T, and P of the Status Register*

A reset condition is initiated by the following events:

1. Power-on condition
2. High-low-high pulse on /RESET pin
3. Watchdog timer time-out
4. When LVR occurs

The values of T and P listed in Table 4 are used to check how the processor wakes up. Table 4 shows the events that may affect the status of T and P.

Table 4 Values of RST, T and P after reset

Reset Type	T	P
Power-on	1	1
/RESET during Operating mode	*P	*P
/RESET wake-up during Sleep mode	1	0
WDT during Operating mode	0	*P
WDT wake-up during Sleep mode	0	0
Wake-up on pin change during Sleep mode	1	0

***P:** *Previous status before reset*

Table 5 Status of T and P Being Affected by Events

Event	T	P
Power-on	1	1
WDTC instruction	1	1
WDT time-out	0	*P
SLEP instruction	1	0
Wake-up on pin change during Sleep mode	1	0

***P:** *Previous value before reset*

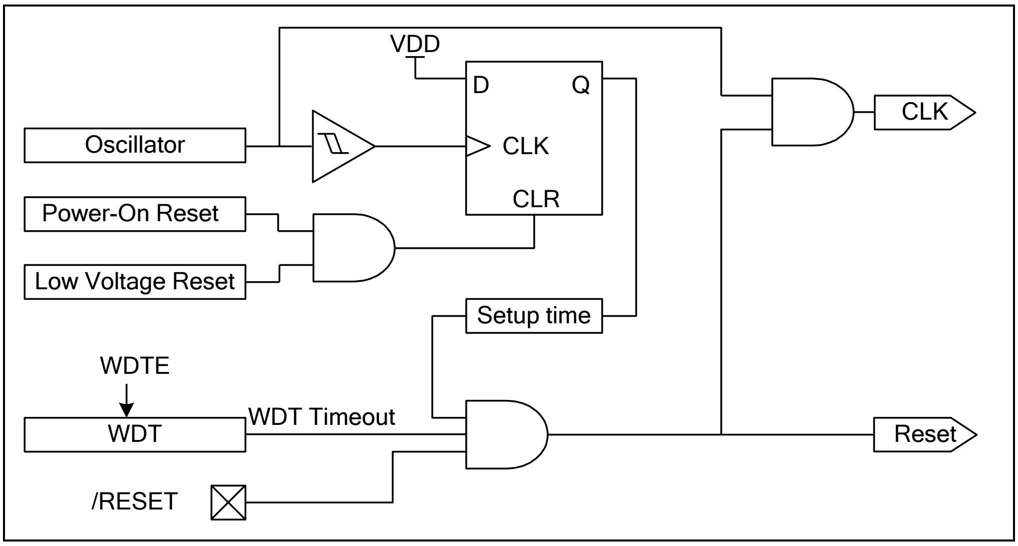


Figure 6-8 Block Diagram of Controller Reset

Table 3 Summary of Register Initial Values after Reset

***Legend: U:** Unknown or don't care* *__P:__ Previous value before reset*
***C:** Same with Code option* ***t:** Check Table 4*

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	Bank 0/1 R0 IAR	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0x01	Bank 0/1 R1 BSR	Bit Name	-	-	-	SBS0	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	P	0	0	0	0
0x02	Bank 0/1 R2 PCL	Bit Name	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0x03	Bank 0/1 R3 SR	Bit Name	INT	N	OV	T	P	Z	DC	C
		Power-on	0	U	U	1	1	U	U	U
		/RESET and WDT	0	P	P	t	t	P	P	P
		Wake-up from Sleep/Idle	P	P	P	t	t	P	P	P
0x04	Bank 0/1 R4 RSR	Bit Name	RSR7	RSR6	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X05	Bank 0 R5 Port 5	Bit Name	P57	P56	P55	P54	P53	P52	P51	P50
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P

(Continuation)

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x06	Bank 0 R6 Port 6	Bit Name	P67	P66	P65	P64	P63	P62	P61	P60
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0x08	Bank 0 R8 Port 8	Bit Name							P81	P80
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0B	Bank 0 RB IOCR5	Bit Name	IOC57	IOC56	IOC55	IOC54	IOC53	IOC52	IOC51	IOC50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0x0C	Bank 0 RC IOCR6	Bit Name	IOC67	IOC66	IOC65	IOC64	IOC63	IOC62	IOC61	IOC60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P

(Continuation)

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0E	Bank 0 RE OMCR	Bit Name	CPUS	IDLE	-	*IIPS*	*FMSF*	*RCM2*	RCM1	RCM0
		Power-on	1	1	0	*0*	0	*C*	C	C
		/RESET and WDT	1	1	0	*0*	0	*C*	C	C
		Wake-up from Sleep/Idle	P	P	*P*	*P*	*P*	*P*	P	P
0x0F	Bank 0 RF EIESCR	Bit Name	-	-	EI32ES1	EI32ES0	EI1ES1	EI1ES0	*EI0ES1*	*EI0ES0*
		Power-on	U	U	*1*	*1*	1	1	1	*1*
		/RESET and WDT	U	U	*1*	*1*	1	1	1	*1*
		Wake-up from Sleep/Idle	*U*	U	*P*	*P*	P	P	*P*	*P*
0x10	Bank 0 R10 WUCR1	Bit Name		*CMPWK*	HLVDWK	ADWK	INTWK1	INTWK0	-	-
		Power-on	0	*0*	*0*	0	0	0	U	U
		/RESET and WDT	0	*0*	*0*	0	0	0	U	U
		Wake-up from Sleep/Idle	*0*	*P*	*P*	P	P	P	U	U
0x11	Bank 0 R11 WUCR2	Bit Name	-	-	-	-	SPIWK	-	-	-
		Power-on	U	U	U	U	0	0	U	U
		/RESET and WDT	U	U	U	U	0	0	U	U
		Wake-up from Sleep/Idle	U	U	U	U	P	0	U	U
0x12	Bank 0 R12 WUCR3	Bit Name	ICWKP8	-	ICWKP6	ICWKP5	-	-	-	INTWK32
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	0	P	P	0	0	0	P
0X14	Bank 0 R14 SFR1	Bit Name	-	*CMPSF*	HLVDSF	ADSF	EXSF1	EXSF0		TCSF
		Power-on	U	*0*	0	0	0	0	0	0
		/RESET and WDT	U	*0*	0	0	0	0	0	0
		Wake-up from Sleep/Idle	U	*P*	P	P	P	P	P	P

(Continuation)

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X15	Bank 0 R15 SFR2	Bit Name	-	-	UERRSF	URSF	UTSF	-	-	TC1DA SF
		Power-on	U	U	0	0	0	0	0	0
		/RESET and WDT	U	U	0	0	0	0	0	0
		Wake-up from Sleep/Idle	U	U	P	P	P	0	0	P
0X16	Bank 0 R16 SFR3	Bit Name					PWMBP SF	PWMBDS F	PWMA PSF	PWMA DSF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	0	P	P	P	P
0X17	Bank 0 R17 SFR4	Bit Name	P8ICSF	-	P6ICSF	P5ICSF	SPISF	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	0	P	P	P	0	0	0
0X18	Bank 0 R18 SFR5	Bit Name							EXSF3	EXSF2
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	0	0	0	P	P
0X19	Bank 0 R19 SFR6	Bit Name	SHSF							TC1DB SF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	0	0	0	0	0	0	P
0X1B	Bank 0 R1B IMR1	Bit Name		CMPIE	HLVDIE	ADIE	EXIE1	EXIE0		
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	P	P	P	P	P	0	0
0X1C	Bank 0 R1C IMR2	Bit Name	-	-	UERRSF	URIE	UTIE	-	-	TC1IE
		Power-on	U	U	0	0	0	0	0	0
		/RESET and WDT	U	U	0	0	0	0	0	0
		Wake-up from Sleep/Idle	U	U	P	P	P	0	0	P

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X1D	Bank 0 R1D IMR3	Bit Name					PWMBPIE	PWMBDIE	PWMAPIE	PWMADIE
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	0	P	P	P	P
0X1E	Bank 0 R1E IMR4	Bit Name	P8ICIE		P6ICIE	P5ICIE	SPIIE			
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	0	P	P	P	0	0	0
0X1F	Bank 0 R1F IMR5	Bit Name							EXIE3	EXIE2
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	0	0	0	P	P
0X20	Bank 0 R20 IMR6	Bit Name	SHIE							
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	0	0	0	0	0	0	0
0X21	Bank 0 R21 WDTCR	Bit Name	WDTE	FSSF			PSWE	WPSR2	WPSR1	WPSR0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	0	0	P	P	P	P
0X24	Bank 0 R24 TC1CR1	Bit Name	TC1S	TC1RC	TC1SS1		TC1FF	TC1OMS	TC1IS1	TC1IS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	0	P	P	P	P
0X25	Bank 0 R25 TC1CR2	Bit Name	TC1M2	TC1M1	TC1M0	TC1SS0	TC1CK3	TC1CK2	TC1CK1	TC1CK0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P

(Continuation)

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X26	Bank 0 R26 TC1DA	Bit Name	TC1DA7	TC1DA6	TC1DA5	TC1DA4	TC1DA3	TC1DA2	TC1DA1	TC1DA0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X27	Bank 0 R27 TC1DB	Bit Name	TC1DB7	TC1DB6	TC1DB5	TC1DB4	TC1DB3	TC1DB2	TC1DB1	TC1DB0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X36	Bank 0 R36 SPICR	Bit Name	CES	SPIE	SRO	SSE	SDOC	SBRS2	SBRS1	SBRS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X37	Bank 0 R37 SPIS	Bit Name	DORD	TD1	TD0	-	OD3	OD4	-	RBF
		Power-on	0	0	0	U	0	0	U	0
		/RESET and WDT	0	0	0	U	0	0	U	0
		Wake-up from Sleep/Idle	P	P	P	U	P	P	U	P
0X38	Bank 0 R38 SPIR	Bit Name	SRB7	SRB6	SRB5	SRB4	SRB3	SRB2	SRB1	SRB0
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X39	Bank 0 R39 SPIW	Bit Name	SWB7	SWB6	SWB5	SWB4	SWB3	SWB2	SWB1	SWB0
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X3A	BANK 0, R3A CMPCR1	Bit Name	CRS	CPOUT	CS1	CS0		CC+S1	CC+S0	SDPWMA
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	0	0	P	P

(Continuation)

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X3B	BANK 0, R3B CMPCR2	Bit Name							CIRL2	SDPWMB
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	0	0	0	0	0	P	P
0X3C	BANK 0, R3C CMPCR3	Bit Name						CIRL1	CIRL0	
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	0	0	0	0	P	P	0
0X3E	Bank 0 R3E ADCR1	Bit Name	CKR2	CKR1	CKR0	ADRUN	ADP	ADOM	SHS1	SHS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X3F	Bank 0 R3F ADCR2	Bit Name	*CALI*	*VPIS2*	ADIM	ADCMS	VPIS1	VPIS0	VREFP	*VREFN*
		Power-on	*0*	*0*	0	0	0	0	0	*0*
		/RESET and WDT	*0*	*0*	0	0	0	0	0	*0*
		Wake-up from Sleep/Idle	*P*	*P*	P	P	P	P	P	*P*
0X40	Bank 0 R40 ADISR	Bit Name	-	-	-	ADIS4	ADIS3	ADIS2	ADIS1	ADIS0
		Power-on	U	U	U	0	0	0	0	0
		/RESET and WDT	U	U	U	0	0	0	0	0
		Wake-up from Sleep/Idle	U	U	U	P	P	P	P	P

(Continuation)

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X41	Bank 0 R41 ADER1	Bit Name	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X42	Bank 0 R42 ADER2	Bit Name	-	-	-	-	ADE11	ADE10	ADE9	ADE8
		Power-on	U	U	U	U	0	0	0	0
		/RESET and WDT	U	U	U	U	0	0	0	0
		Wake-up from Sleep/Idle	U	U	U	U	P	P	P	P
0X43	Bank 0 R43 ADDL	Bit Name	ADD7	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	U	U	U	U	U	U	U	U
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X44	Bank 0 R44 ADDH	Bit Name	ADD15	ADD14	ADD13	ADD12	ADD11	ADD10	ADD9	ADD8
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	U	U	U	U	U	U	U	U
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X45	Bank 0 R45 ADCVL	Bit Name	ADCV7	ADCV6	ADCV5	ADCV4	ADCV3	ADCV2	ADCV1	ADCV0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X46	Bank 0 R46 ADCVH	Bit Name	ADCV15	ADCV14	ADCV13	ADCV12	ADCV11	ADCV10	ADCV9	ADCV8
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P

(Continuation)

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X05	Bank 1 R5 IOCR8	Bit Name							IOC81	IOC80
		Power-on	0	0	0	0	0	0	1	1
		/RESET and WDT	0	0	0	0	0	0	1	1
		Wake-up from Sleep/Idle	0	0	0	0	0	0	P	P
0X08	Bank 1 R8 P5PHCR	Bit Name	PH57	PH56	PH55	PH54	PH53	PH52	PH51	PH50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X09	Bank 1 R9 P6PHCR	Bit Name	PH67	PH66	PH65	PH64	PH63	PH62	PH61	PH60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0A	Bank 1 RA P8PHCR	Bit Name						P8LPH		
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0B	Bank 1 RB P5PLCR	Bit Name	PL57	PL56	PL55	PL54	PL53	PL52	PL51	PL50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P

(Continuation)

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X0C	Bank 1 RC P6PLCR	Bit Name	PL67	PL66	PL65	PL64	PL63	PL62	PL61	PL60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0D	Bank 1 RD P8PLCR	Bit Name						P8LPL		
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0E	Bank 1 RE P5HDSCR	Bit Name	HDS57	HDS56	HDS55	HDS54	HDS53	HDS52	HDS51	HDS50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0F	Bank 1 RF P6HDSCR	Bit Name	HDS67	HDS66	HDS65	HDS64	HDS63	HDS62	HDS61	HDS60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X10	Bank 1 R10 P8HDSCR	Bit Name						P8LHDS		
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X11	Bank 1 R11 P5ODCR	Bit Name	OD57	OD56	OD55	OD54	OD53	OD52	OD51	OD50
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X12	Bank 1 R2 P6ODCR	Bit Name	OD67	OD66	OD65	OD64	OD63	OD62	OD61	OD60
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P

(Continuation)

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X13	Bank 1 R13 P8ODCR	Bit Name						P8LOD		
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X14	BANK 1, R14 DeadTCR	Bit Name					DEADTBE	DEADTAE	DEADTP1	DEADTP0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	0	0	0	P	P	P	P
0X15	BANK 1, R15 DeadTR	Bit Name					DEADTR3	DEADTR2	DEADTR1	DEADTR0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	0	0	0	P	P	P	P
0X16	BANK 1, R16 PWMSCR	Bit Name				DEADS			PWMBS	PWMAS
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	0	0	P	0	0	P	P
0X17	BANK 1, R17 PWMACR	Bit Name	PWMAE	IPWMAE	PWMAA	IPWMAA	TAEN	TAP2	TAP1	TAP0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X18	BANK 1, R18 PRDAL	Bit Name	PRDA7	PRDA6	PRDA5	PRDA4	PRDA3	PRDA2	PRDA1	PRDA0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X19	BANK 1, R19 PRDAH	Bit Name							PRDA9	PRDA8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	0	0	0	0	0	P	P
0X1A	BANK 1, R1A DTAL	Bit Name	DTA7	DTA6	DTA5	DTA4	DTA3	DTA2	DTA1	DTA0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P

(Continuation)

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X1B	BANK 1, R1B DTAH	Bit Name							DTA9	DTA8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	0	0	0	0	0	P	P
0X1C	BANK 1, R1C TMRAL	Bit Name	TMRA7	TMRA6	TMRA5	TMRA4	TMRA3	TMRA2	TMRA1	TMRA0
		Power-On	0	0	0	0	0	0	0	1
		/RESET and WDT	0	0	0	0	0	0	0	1
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X1D	BANK 1, R1D TMRAH	Bit Name							TMRA9	TMRA8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	0	0	0	0	0	P	P
0X1E	BANK 1, R1E PWMBCR	Bit Name	PWMBE	IPWMBE	PWMBA	IPWMBA	TBEN	TBP2	TBP1	TBP0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X1F	BANK 1, R1F PRDBL	Bit Name	PRDB7	PRDB6	PRDB5	PRDB4	PRDB3	PRDB2	PRDB1	PRDB0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X20	BANK 1, R20 PRDBH	Bit Name							PRDB9	PRDB8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	0	0	0	0	0	P	P
0X21	BANK 1, R21 DTBL	Bit Name	DTB7	DTB6	DTB5	DTB4	DTB3	DTB2	DTB1	DTB0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	0	0	0	P	P	P	P
0X22	BANK 1, R22 DTBH	Bit Name							DTB9	DTB8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	0	0	0	0	0	P	P

(Continuation)

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X23	BANK 1, R23 TMRBL	Bit Name	TMRB7	TMRB6	TMRB5	TMRB4	TMRB3	TMRB2	TMRB1	TMRB0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X24	BANK 1, R24 TMRBH	Bit Name							TMRB9	TMRB8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	0	0	0	0	0	P	P
0X33	Bank 1 R33 URCR	Bit Name	UINVEN	UMODE1	UMODE0	BRATE2	BRATE1	BRATE0	UTBE	TXE
		Power-on	0	0	0	0	0	0	1	0
		/RESET and WDT	0	0	0	0	0	0	1	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X34	Bank 1 R34 URS	Bit Name	URTD8	EVEN	PRE	PRERR	OVERR	FMERR	URBF	RXE
		Power-on	U	0	0	0	0	0	0	0
		/RESET and WDT	P	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X35	Bank 1 R35 URTD	Bit Name	URTD7	URTD6	URTD5	URTD4	URTD3	URTD2	URTD1	URTD0
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X36	Bank 1 R36 URRDL	Bit Name	URRD7	URRD6	URRD5	URRD4	URRD3	URRD2	URRD1	URRD0
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X37	Bank 1 R37 URRDH	Bit Name	URRD8	-	-	-	-	-	-	URSS
		Power-on	U	U	U	U	U	U	U	*U*
		/RESET and WDT	P	U	U	U	U	U	U	*P*
		Wake-up from Sleep/Idle	P	U	U	U	U	U	U	*P*

(Continuation)

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X45	Bank 1 R45 TBPTL	Bit Name	TB7	TB6	TB5	TB4	TB3	TB2	TB1	TB0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X46	Bank 1 R46 TBPTH	Bit Name	HLB	GP	GP	GP	TB11	TB10	TB9	TB8
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X47	Bank 1 R47 STKMON	Bit Name	STOV	-	-	-	STL3	STL2	STL1	STL0
		Power-on	0	U	U	U	0	0	0	0
		/RESET and WDT	0	U	U	U	0	0	0	0
		Wake-up from Sleep/Idle	P	U	U	U	P	P	P	P
0X48	Bank 1 R48 PCH	Bit Name	-	-	-	-	PC11	PC10	PC9	PC8
		Power-on	U	U	U	*U*	0	0	0	0
		/RESET and WDT	U	U	U	*U*	0	0	0	0
		Wake-up from Sleep/Idle	U	U	U	*U*	P	P	P	P
0X49	Bank 1 R49 HLVDCR	Bit Name	HLVDEN	IRVSF	VDSB	VDM	HLVDS3	*HLVDS2*	*HLVDS1*	*HLVDS0*
		Power-on	0	0	1	0	1	*1*	*1*	*1*
		/RESET and WDT	0	0	1	0	1	*1*	*1*	*1*
		Wake-up from Sleep/Idle	P	P	P	P	P	*P*	*P*	*P*
0X50 ~ 0X7F	Bank 0 R50~R7F	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X80 ~ 0XFF	Bank 0~3 R80~RFF	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P

6.5 Interrupt

The EM88F712N has 15 interrupts (4 external, 11nternal) as listed below:

Interrupt Source		Enable Condition	Int. Flag	Int. Vector	Priority
Internal/External	Reset	-	-	0	High 0
External	INT	ENI + EXIE=1	EXSF	2	1
External	Pin change	ENI +ICIE=1	ICSF	4	2
Internal	HLVD	ENI+HLVDEN & HLVDIE=1	HLVDSF	8	3
External	Comparator	ENI+CMPIE=1	CMPSF	A	4
Internal	SPI	ENI + SPIIE=1	SPISF	C	5
Internal	AD	ENI + ADIE=1	ADSF	10	6
Internal	TC1	ENI + TC1IE=1	TC1DASF TC1DBSF	12	7
Internal	PWMPA	ENI+PWMPAIE=1	PWMPASF	14	8
Internal	PWMDA	ENI+PWMDAIE=1	PWMDASF	16	9
Internal	PWMPB	ENI+PWMPBIE=1	PWMPBSF	24	10
Internal	PWMDB	ENI+PWMDBIE=1	PWMDBSF	26	11
Internal	UART Receive error	ENI+UERRIE=1	UERRSF	2E	12
Internal	UART Receive	ENI + URIE=1	URSF	30	13
Internal	UART Transmit	ENI + UTIE=1	UTSF	32	14
External	System hold	ENI + SHIE=1	SHSF	34	15

Bank 0 R15~R1A are the interrupt status registers that record the interrupt requests in relative flags/bits. Bank 0 R1B~R20 is the Interrupt Mask register. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. When one of the enabled interrupts occurs, the next instruction will be fetched from their individual addresses. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine and before interrupts are enabled to avoid recursive interrupts.

The flag (except ICSF bit delete) in the Interrupt Status Register is set regardless of the status of its mask bit or the execution of ENI. The RETI instruction ends the interrupt routine and enables the global interrupt (the execution of ENI).

External interrupt is equipped with digital noise rejection circuit (input pulse of less than **4 system clock time** is eliminated as noise), **but in Low XTAL oscillator (LXT) mode, the noise rejection circuit is disabled**. When an interrupt (Falling edge) is generated by the External interrupt (when enabled), the next instruction will be fetched from Address 0X02H.

Before the interrupt subroutine is executed, the contents of ACC, R3 (Bit 0~Bit 4) and R4 registers are saved by hardware. If another interrupt occurs, the ACC, R3 (Bit 0~Bit 4) and R4 registers will be replaced by the new interrupt. After the interrupt service routine is finished, ACC, R3 (Bit 0~Bit 4) and R4 are restored.

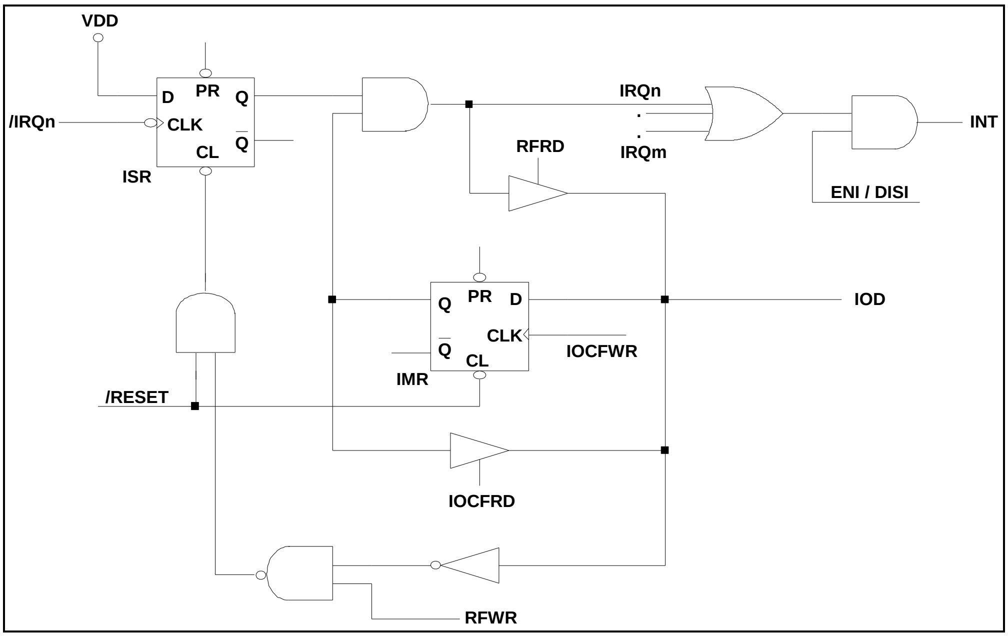


Figure 6-9a Interrupt Input Circuit

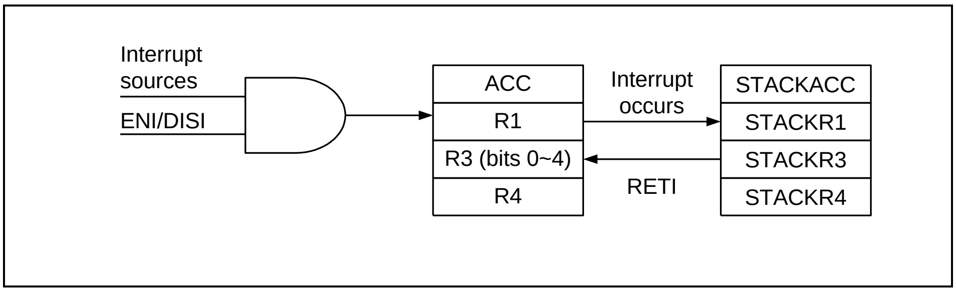


Figure 6-9b Interrupt Backup Diagram

6.6 A/D Converter

R_BANK	Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 0	0x3E	ADCR1	CKR2	CKR1	CKR0	ADRUN	ADP	ADOM	SHS1	SHS0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x3F	ADCR2	-	VPIS2	ADIM	ADCMS	VPIS1	VPIS0	VREFP	VREFN
			-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x40	ADISR	-	-	-	ADIS4	ADIS3	ADIS2	ADIS1	ADIS0
			-	-	-	R/W	R/W	R/W	R/W	R/W
Bank 0	0x41	ADER1	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x42	ADER2	-	-	-	-	ADE11	ADE10	ADE9	ADE8
			-	-	-	-	R/W	R/W	R/W	R/W
Bank 0	0x43	ADDL	ADD7	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0
			R	R	R	R	R	R	R	R
Bank 0	0x44	ADDH	ADD15	ADD14	ADD13	ADD12	ADD11	ADD10	ADD9	ADD8
			R	R	R	R	R	R	R	R
Bank 0	0x45	ADCVL	ADCD7	ADCD6	ADCD5	ADCD4	ADCD3	ADCD2	ADCD1	ADCD0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x46	ADCVH	ADCD15	ADCD14	ADCD13	ADCD12	ADCD11	ADCD10	ADCD9	ADCD8
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x10	WUCR2	-	-	-	ADWK	-	-	-	-
			-	-	-	R/W	-	-	-	-
Bank 0	0x15	SFR1	-	-	-	ADSF	-	-	-	-
			-	-	-	R/W	-	-	-	-
Bank 0	0x1B	IMR1	-	-	-	ADIE	-	-	-	-
			-	-	-	R/W	-	-	-	-

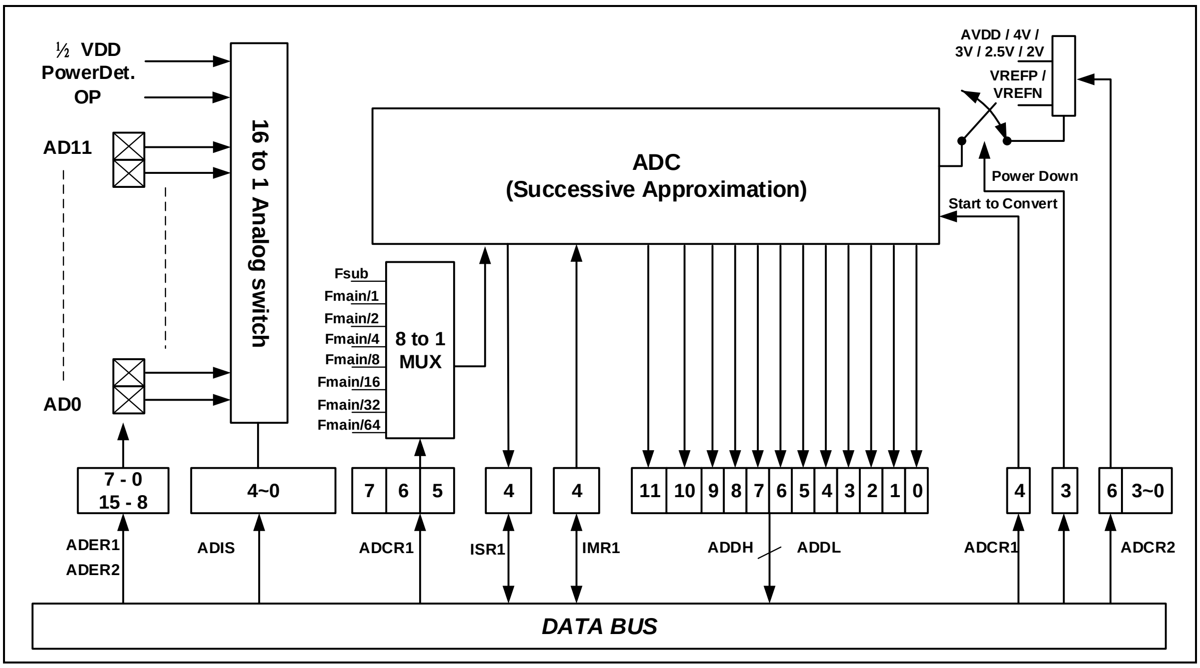


Figure 6-10 ADC Functional Block Diagram

This is a 12-bit successive approximation register analog-to-digital converter (SAR ADC). There are two reference voltages for SAR ADC. The positive reference voltage can select internal AVDD, internal voltage sources or external input pin by setting the VREFN, VREFP and VPIS2~0 bits in ADCR2. Connecting to external positive reference voltage provides more accuracy than using internal AVDD.

6.6.1 ADC Data Register

When the AD conversion is completed, the result is loaded to the ADDH and ADDL. And the ADSF is set if ADIE is enabled.

6.6.2 A/D Sampling Time

The accuracy, linearity, and speed of the successive approximation AD converter are dependent on the properties of the ADC. The source impedance and the internal sampling impedance directly affect the time required to charge the sample and hold capacitor. The application program controls the length of the sample time to meet the specified accuracy. The maximum recommended impedance for the analog source is 10kΩ at VDD = 5V. After the analog input channel is selected, this acquisition time must be done before AD conversion can be started.

6.6.3 A/D Conversion Time

CKR2~0 select the conversion time (TAD). This allows the MCU to run at maximum frequency without sacrificing the accuracy of AD conversion. The following tables show the relationship between T_{AD} and the maximum operating frequencies. The T_{AD} is 0.5 µs for 3V~5.5V and T_{AD} is 2 µs for 2.5V~3V.

System Mode	CKR[2:0]	Operating Clock of ADC ($F_{AD} = 1 / T_{AD}$)	Max. F_{Main} (V_{DD} = 3V ~ 5.5V)	Max. F_{Main} (V_{DD} = 2.5V ~ 3V)
Normal Mode	000	F_{Main} / 16	16 MHz	8 MHz
	001	F_{Main} / 8	16 MHz	4 MHz
	010	F_{Main} / 4	8 MHz	2 MHz
	011	F_{Main} / 2	4 MHz	1 MHz
	100	F_{Main} / 64	16 MHz	16 MHz
	101	F_{Main} / 32	16 MHz	16 MHz
	110	F_{Main} / 1	2 MHz	0.5 MHz
	111	F_{Sub}	Fs	Fs
Green Mode	xxx	F_{Sub}	Fs	Fs

***** Conversion Time = Sample and Hold (SHS[1:0]=10, 8 * T_{AD}) + 12 * Bit Conversion Time (12 * T_{AD}) + Delay Time between setting ADSTART bit and starting first T_{AD}.

6.6.4 ADC Operation during Sleep Mode

In order to obtain a more accurate ADC value and reduce power consumption, the AD conversion remains operational during sleep mode. As the SLEP instruction is executed, all the MCU operations will stop except for the Oscillator, TC1, PWMA~C and AD conversion.

The AD Conversion is considered completed as determined by:

1. The ADRUN bit of the Bank 0-R3E register is cleared to “0”.
2. The ADSF bit of the Bank 0-R14 register is set to “1”.
3. The ADWK bit of the Bank 0-R10 register is set to “1” and wakes up from ADC conversion (where it remains in operation during sleep mode).
4. Wake-up and execution of the next instruction if the ADIE bit of the Bank 0-R1B is enabled and the “DISI” instruction is executed.
5. Wake up and enter into interrupt vector if the ADIE bit of Bank 0-R1B is enabled and the “ENI” instruction is executed.
6. Enter into an interrupt vector if the ADIE bit of the Bank 0-R1B is enabled and the “ENI” instruction is executed.

The results are fed into the ADDL and ADDH registers when the conversion is completed. If the ADWK is enabled, device will wake up. Otherwise, the AD conversion will be shut off, no matter what the status of the ADP bit is.

6.6.5 Programming Process/Considerations

Follow these steps to obtain data from the ADC:

1. **AD pins that are not data-converted must be set as high-impedance inputs and can not be set as output pins (Pull-High or Pull-Low).**
2. Write to the ADCR1/ADCR2 register to configure the AD module:
   a) Define the AD conversion clock rate (CKR2~0)
   b) Select the VREFS input source of the ADC
   c) Set the ADP bit to “1” to begin sampling
3. **Select the ADC input channel (ADIS4~0)**
4. **Enable the corresponding AD conversion pin (ADER1~2) to the ADC input channel selected in Step 3.**
5. If the wake-up function is used, set the ADWK bit to "1".
6. If the interrupt function is used, set the ADIE bit to "1".
7. If the interrupt function is used, set an "ENI" instruction.
8. Set the ADRUN bit to **“1”**
9. Write “SLEP” instruction or Polling.

10. Wait for either Wake-up or for the ADRUN bit to be cleared to "**0**", and the Status flag (ADSF) is set "**1**", or ADC interrupt occurs.

11. Read the ADDL and ADDH conversion data registers. If the ADC input channel changes at this time, the ADDL and ADDH values can be cleared to "**0**".

12. Clear the status flag (ADSF).

13. Turn off the selected AD conversion pin function (ADER1~2).

14. If necessary, proceed to the next conversion program and jump to Step 3 or 4. At least two T_{AD} are required before the next acquisition starts. On the other hand, the timing setting ADRUN = 1 must be later than the timing setting ADP=1, and the difference between the two timing is also two T_{AD}.

For actual program settings, refer to the section in red in the program demonstration.

If the procedure described above is not followed, the AD conversion value may not come out as expected.

※ **Note:**

1. In order to obtain accurate values, it is necessary to avoid any data transfer in I/O pins during AD conversion.

2. Order of setting the register
   - **Before setting the AD conversion pins (ADER1~2), the corresponding input channel (ADISR) and ADC power supply (ADP = 1) must be set.**
   - **After the AD conversion is completed, turn off the AD conversion pin function (ADER1~2).**

3. **AD pins that are not data-converted must be set as high-impedance input pins.** For example, if P52, P53, and P54 (AD0~2) are AD pins, P53 and P54 must be set as high-impedance input pins to begin P53 AD data conversion. Similarly, to begin P53 AD data conversion, P52 and P54 must be set as high-impedance input pins. [P52, P53, and P54 can be set as high-impedance input pins during program initialization]

6.6.6 Programming Process for Detecting Internal VDD

VDD is detected within the operation, as described in the previous section, the difference is that before starting the ADC conversion, the first detection of VDD is ready. Therefore, in detecting VDD:

It should be noted that before starting the AD conversion operation, the channel has to be switched to 1/2VDD, the voltage divider needs to be started before AD can be converted. Several points to note is that, precise conversion values can be added in the VDD Pin capacitance, or more than twice the conversion, taking the average of the last few strokes data in order to increase the reliability of the data.

Note that usually before VDD is detected, do not switch the channel to 1/2VDD. As there has always been a DC current consumption, the channel must be switched to another channel analog multiplexer, and it will be shut out of the resistor divider. User attention is required.

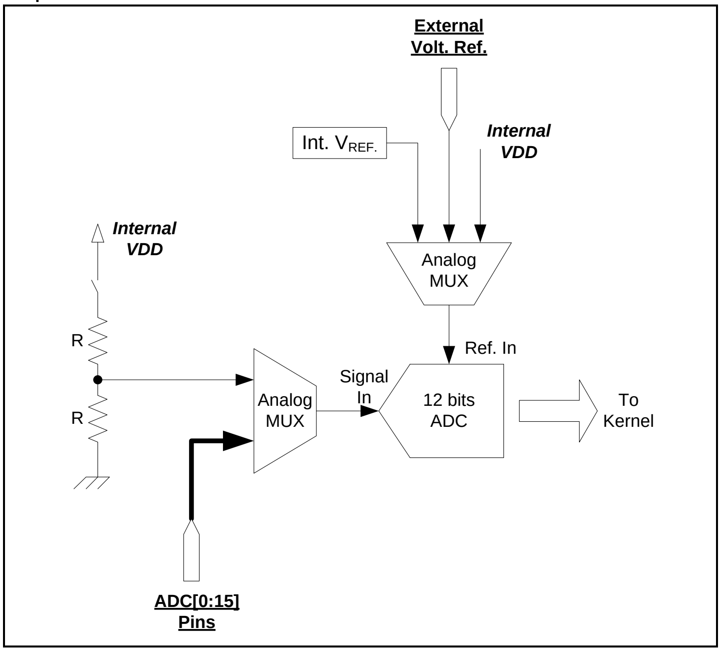


Figure 6-11 ADC and VDD Detection Block Diagram

6.6.7 Sample Demo Programs

The following is an example of the use of ADC function, demonstrating a single data conversion. Users can make different settings according to demand.

A. Define System Control Registers

```
IAR    == 0X00          ; Indirect addressing register
SR     == 0X03          ; Status register
WUCR1  == 0x10          ; Wakeup Control Register 1
     ADWK  == WUCR1.4
SFR1   == 0x14          ; Status Flag Register 1
     ADSF  == SFR1.4
IMR1   == 0x1B          ; Interrupt Mask Register 1
     ADIE  == IMR1.4
```

B. Define I/O Control Registers

```
PORT5 == 0X05
IOCR5 == 0x0B           ; I/O Control Register of Port 5
```

C. ADC Control Register

```
ADCR1 == 0x3E           ; ADC Control Register 1
     CKR2   == ADCR1.7
     CKR1   == ADCR1.6
     CKR0   == ADCR1.5
     ADRUN  == ADCR1.4
     ADP    == ADCR1.3
     ADOM   == ADCR1.2
     SHS1   == ADCR1.1
     SHS0   == ADCR1.0
ADISR == 0x40           ; ADC input Channel select register
ADER1 == 0x41           ; ADC Input Control Register 1
ADER2 == 0x42           ; ADC Input Control Register 2
ADDL  == 0x43           ; The contents are the results of ADC[7:0]
ADDH  == 0x44           ; The contents are the results of ADC[11:8]
```

D. Define General Register

```
ADCTMP0 == 0x50         ;
ADCTMP1 == 0x51         ;
```

E. Program Starts

```
ORG  0x00               ; Initial address
JMP  INITIAL            ;
```

```
ORG   0x12                ; ADC Interrupt vector
JMP   ADC_Int
;
; (User program section)
;
ADC_Int:
MOV   A, ADDH             ; To read high byte of AD data buffer
MOV   ADCTMP0,A
MOV   A, ADDL             ; To read low byte of AD data buffer
MOV   ADCTMP1,A
BC    ADSF                ; To clear the ADSF bit
BC    ADER1, 2            ; Disable P54(AD2) to act as analog
                          ; input pin
RETI

INITIAL:
MOV   A,@0xFF             ; To define PORT5 as an input pin
MOV   IOCR5, A

MOV   A, @0B00001000      ; AD power on (ADP=1), and set clock
                          ; rate at fosc/16
MOV   ADCR1, A
BS    ADWK                ; Enable the ADWK wake-up function of ADC
BS    ADIE                ; Enable the ADIE interrupt function
ENI                       ; Enable the interrupt function

En_ADC:;                  ;
MOV   A, @0x02            ; To define AD2 as an analog input
MOV   ADISR, A
BS    ADER1, 2            ; To Enable P54(AD2) as an analog
                          ; input channel
BS    ADRUN               ; Start to run the ADC
SLEP

; If the interrupt function is employed, the following nine lines
may be ignored
;
; (User program section)
```

```
;
POLLING:
JBS   ADSF            ; To check the ADSF bit continuously
JMP   POLLING         ; ADRUN bit will be set 1 as the AD conversion
                      ; is completed
MOV   A, ADDH         ; To read high byte of AD data buffer
MOV   ADCTMP0,A
MOV   A, ADDL         ; To read low byte of AD data buffer
MOV   ADCTMP1,A
BC    ADSF            ; To clear the ADSF bit

BC    ADER1, 2        ; Disable P54(AD2) to act as analog input pin
```

6.7 Timer

Timer 1 can be one 8-bit up-counter.

R_BANK	Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 0	0x24	TC1CR1	TC1S	TC1RC	TC1SS1	TC1MOD	TC1FF	TC1OMS	TC1IS1	TC1IS0
			R/W	R/W	R/W	R/W	R	R/W	R/W	R/W
Bank 0	0x25	TC1CR2	TC1M2	TC1M1	TC1M0	TC1SS0	TC1CK3	TC1CK2	TC1CK1	TC1CK0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x26	TC1DA	TC1DA7	TC1DA6	TC1DA5	TC1DA4	TC1DA3	TC1DA2	TC1DA1	TC1DA0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x27	TC1DB	TC1DB7	TC1DB6	TC1DB5	TC1DB4	TC1DB3	TC1DB2	TC1DB1	TC1DB0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x15	SFR2	-	-	-	-	-	-	-	TC1DASF
			-	-	-	-	-	-	-	F
Bank 0	0x19	SFR6	-	-	-	-	-	-	-	TC1DBSF
			-	-	-	-	-	-	-	F
Bank 0	0x1C	IMR2	-	-	-	-	-	-	-	TC1DIE
			-	-	-	-	-	-	-	R/W

6.7.1 Timer/Counter Mode

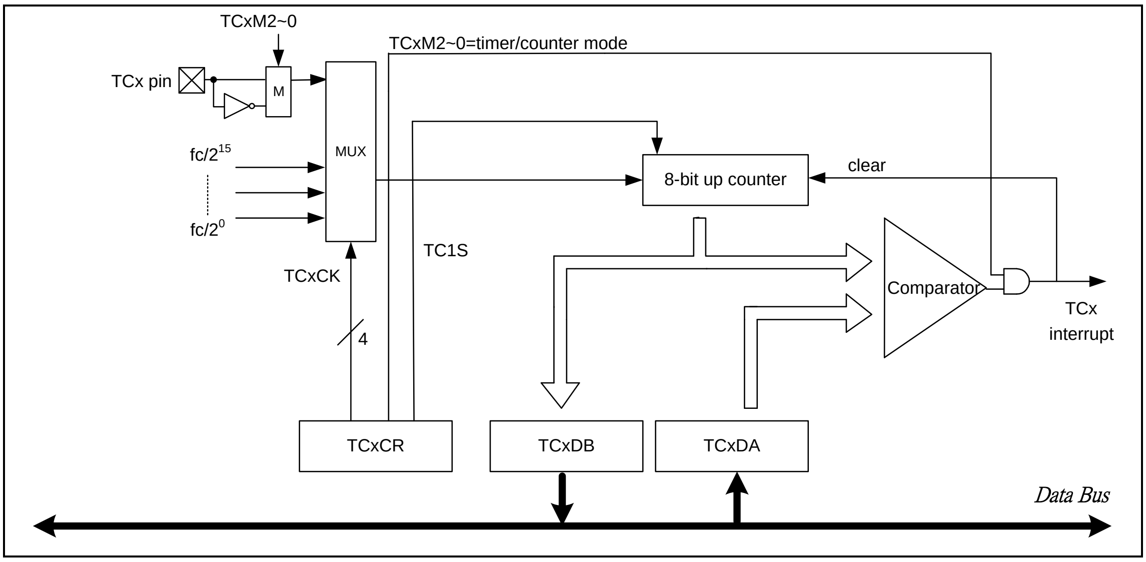


Figure 6-12a Timer/Counter Mode Block Diagram

In Timer/Counter mode, counting up is performed using internal clock or TCx pin. When the contents of the up-counter are matched with the TCxDA, interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared. The current contents of the up-counter are loaded into TCxDB by setting TCxRC to "1".

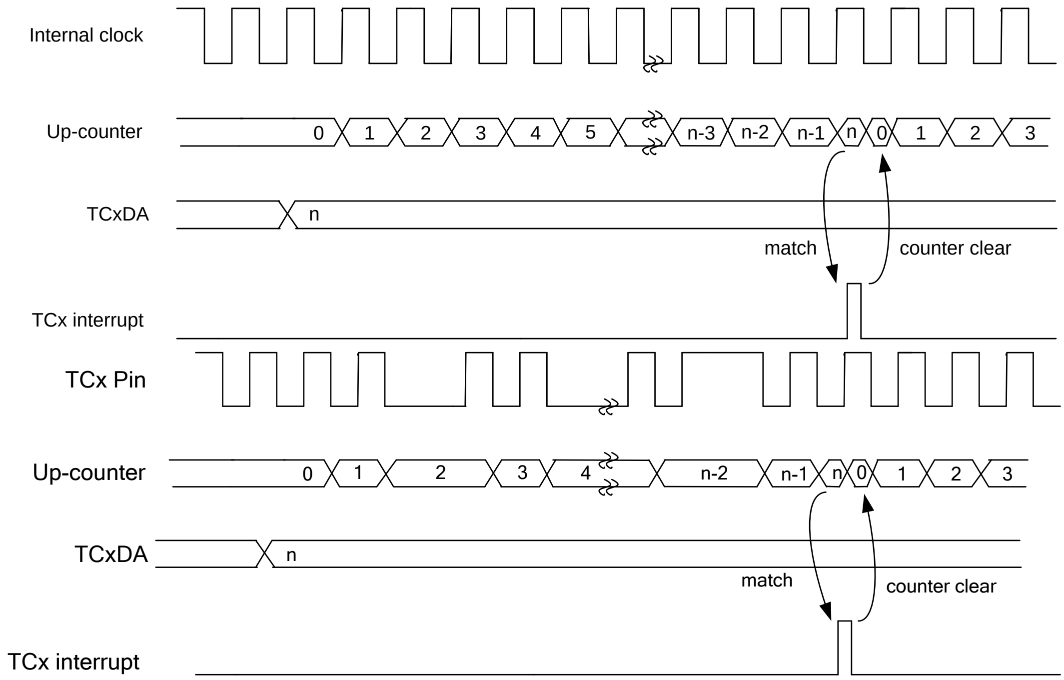


Figure 6-12b Timer/Counter Mode Waveform

6.7.2 Window Mode

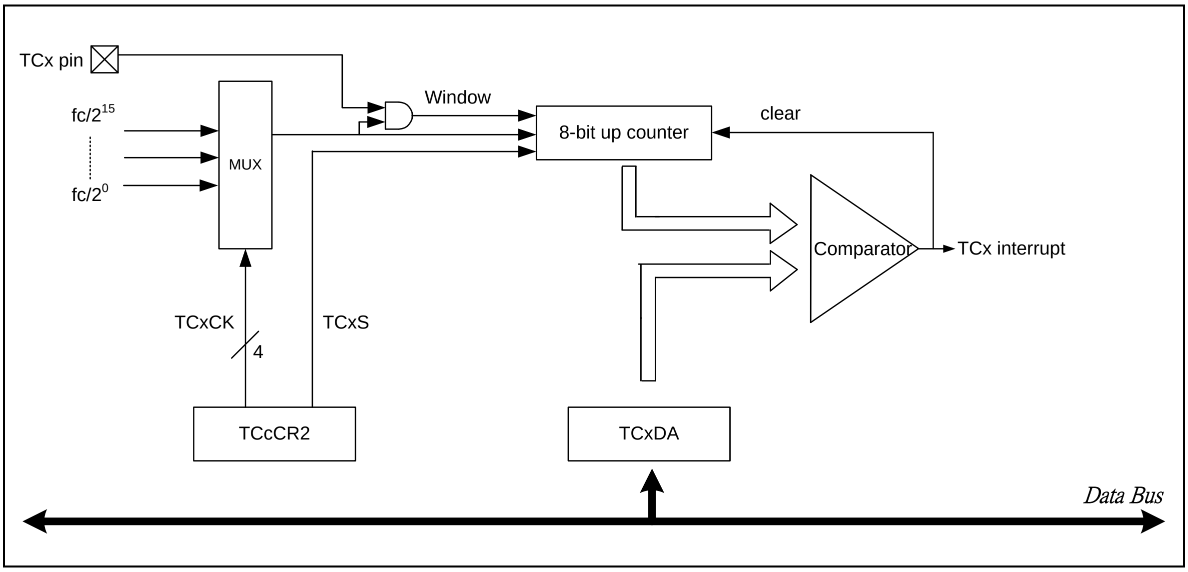


Figure 6-13a Window Mode Block Diagram

In Window mode, counting up is performed on a rising edge of the pulse that is logical AND of an internal clock and the TCx pin (window pulse). When the contents of the up-counter match with the TCxDA, interrupt is generated and the counter is cleared. The frequency (window pulse) must be lower than the selected internal clock.

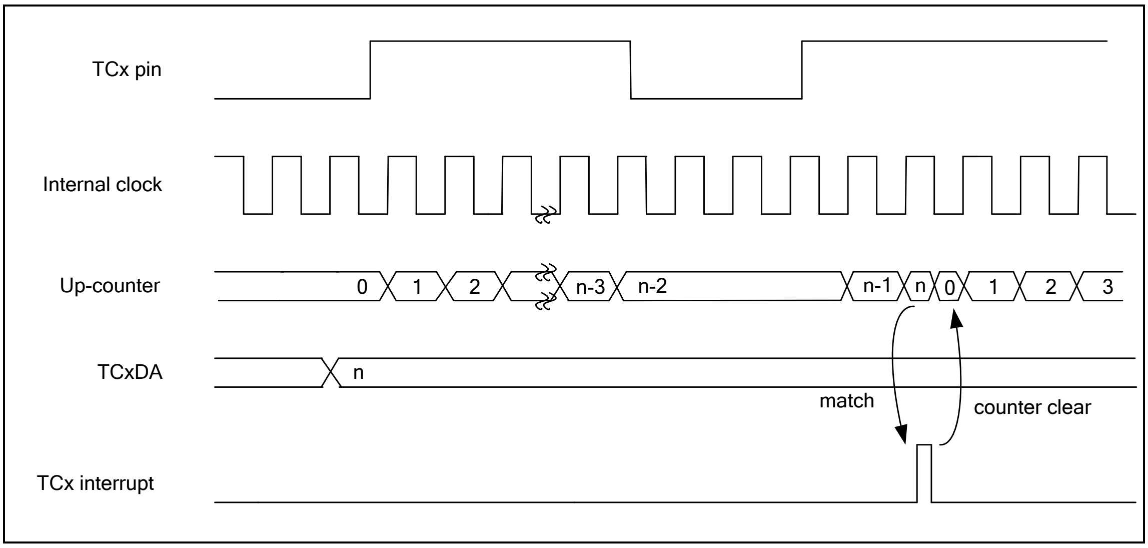


Figure 6-13b Window Mode Waveform

6.7.3 Capture Mode

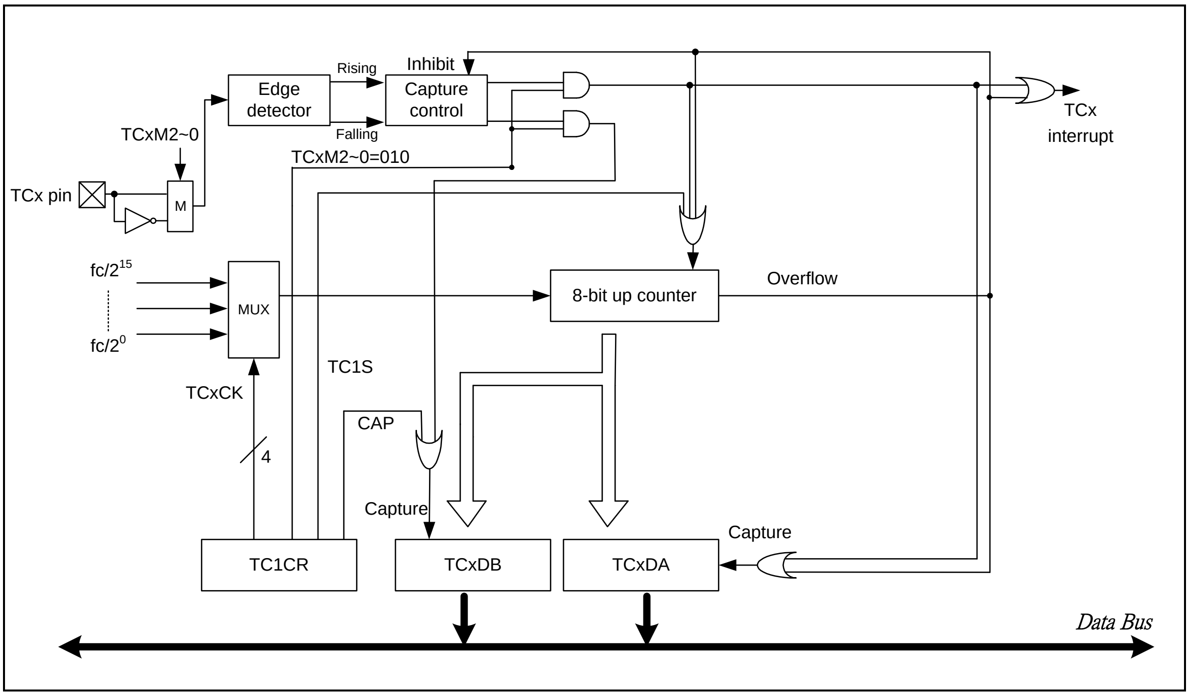


Figure 6-14a Capture Mode Block Diagram

In Capture mode, the pulse width, period and duty of the TCx input pin are measured and can be used to decode the remote-control signal. The counter is free running by the internal clock. On a rising (falling) edge of TCx pin, the contents of the counter are loaded into TCxDA, then the counter is cleared and interrupt is generated. On a falling (rising) edge of TC1 pin, the contents of the counter are loaded into TCxDB. At this time, the counter is still counting. Once the next rising edge of TCx pin is triggered, the contents of the counter are loaded into TCxDA, the counter is cleared and interrupt is generated again. If overflow before the edge is detected, the FFH is loaded into TCxDA and an overflow interrupt is generated. During interrupt processing, it can be determined whether or not there is an overflow by checking if the TCxDA value is FFH. After an interrupt (capture to TCxDA or overflow detection) is generated, capture and overflow detection are halted until TCxDA is read out.

(1) normal action
(2) can not be interrupted
(3) signal less than 2 timer clk can not be identified
(4) DA overflow
(5) DB overflow
(6) DB overflow after the need for signal rise edge will be re-counted

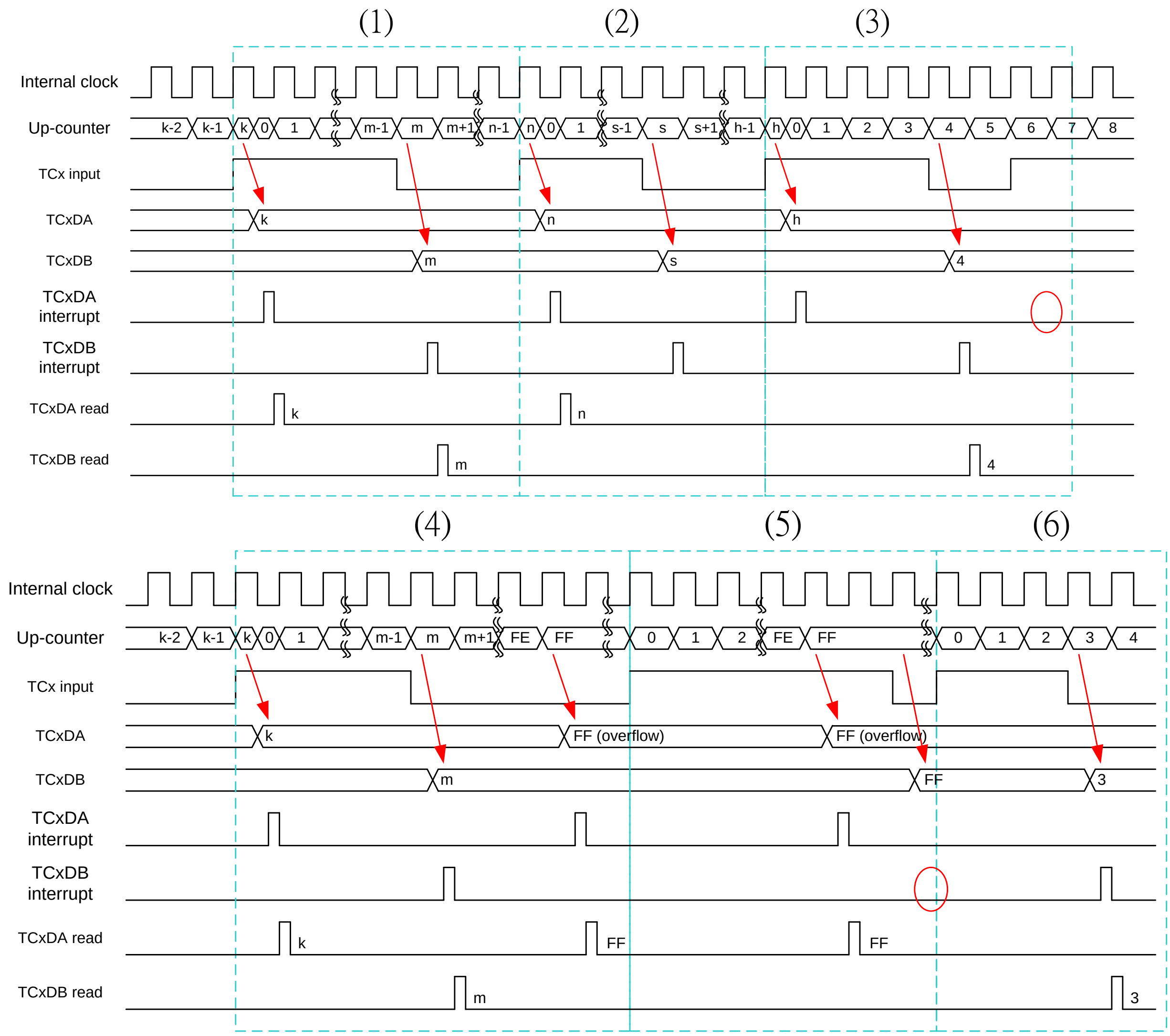


Figure 6-14b Capture Mode Waveform

6.7.4 Programmable Divider Output Mode and Pulse Width Modulation Mode

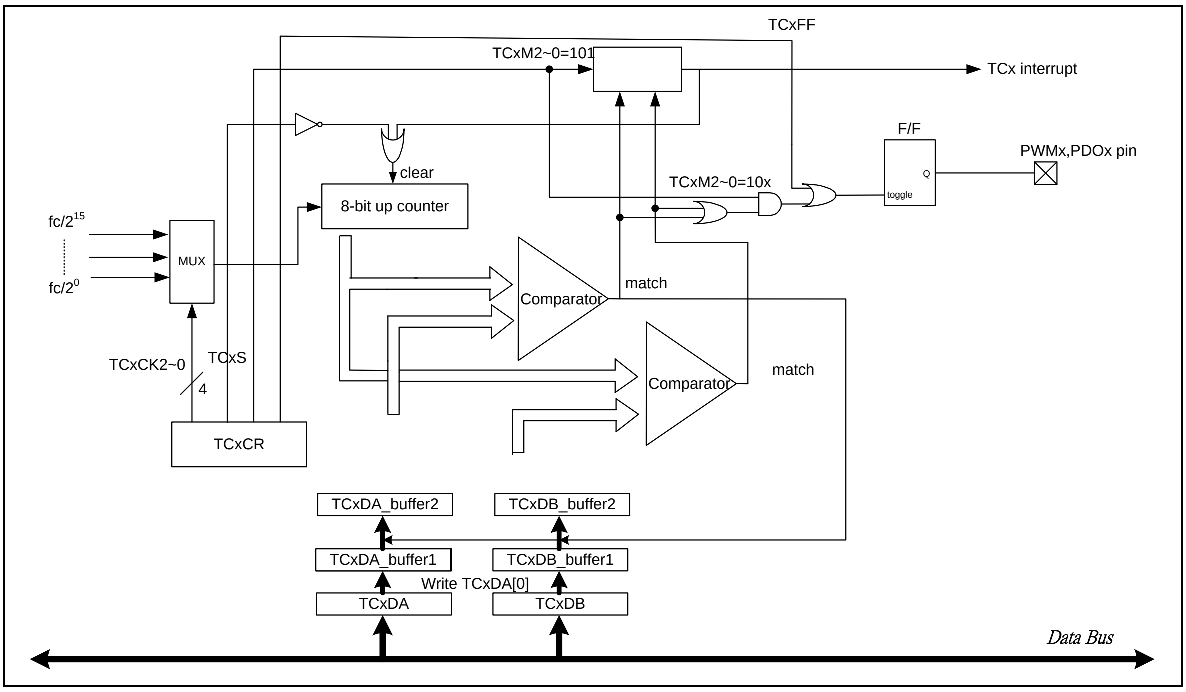


Figure 6-15a PDO/PWM Mode Block Diagram

- **Programmable Divider Output (PDO)**

In Programmable Divider Output (PDO) mode, counting up is performed using the internal clock. The contents of TCxDA are compared with the contents of the up-counter. The F/F output is toggled and the counter is cleared each time a match is found. The F/F output is inverted and output to PDO pin. This mode can generate 50% of duty pulse output. The PDO pin is initialized to "**0**" during reset. A TCx interrupt is generated each time the PDO output is toggled.

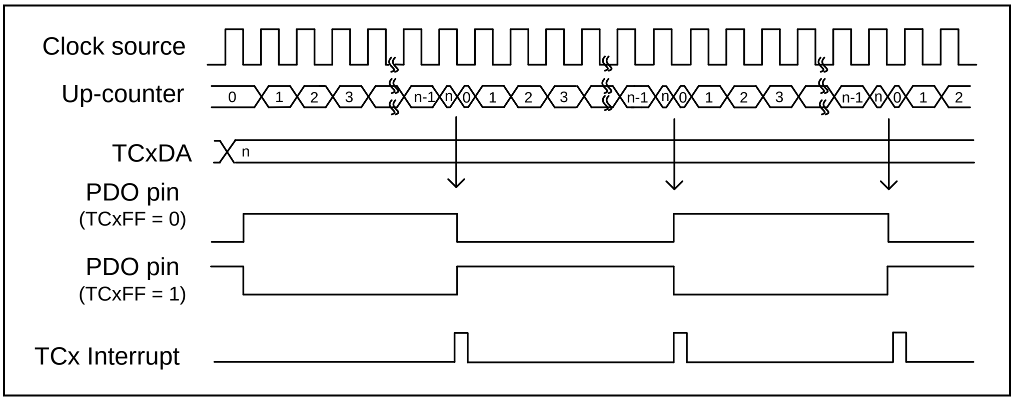


Figure 6-15b PDO Mode Waveform

- **Pulse Width Modulation (PWM)**

In Pulse Width Modulation (PWM) Output mode, counting up is performed using the internal clock with prescaler. The Duty of PWMx is controlled by TCxDB, and the period of PWMx is controlled by TCxDA. Pulse at the PWMx pin is held to high level as long as TCxS=1 or timerx matches TCxDA; meanwhile the pulse is held to low level as long as Timerx matches TCxDB. Once TCxFF is set to 1, PWMx signal is inverted, a TCx interrupt is generated and defined by TCxIS. On the other hand, although TCxDA and TCxDB can be written anytime, the data of TCxDA and TCxDB are latched only when writing TCxDA0. Therefore, new duty and new period of PWM appear at the PMW pin in the last period–match.

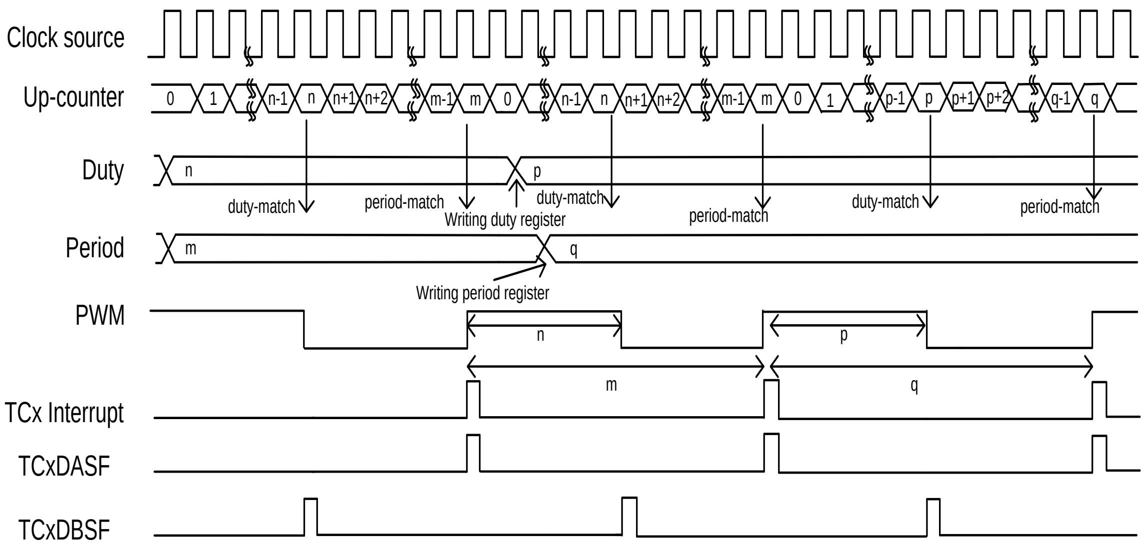


Figure 6-15c PWM Mode Waveform

6.7.5 Buzzer Mode

The TCx pin outputs the clock after dividing the frequency.

6.8 PWM (Pulse Width Modulation)

R_BANK	Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 0	0x16	SFR3					PWMBPSF	PWMBDSF	PWMAPSF	PWMADSF
							F	F	F	F
Bank 0	0x1D	IMR3					PWMBPIE	PWMBDIE	PWMAPIE	PWMADIE
							R/W	R/W	R/W	R/W
Bank 1	0x14	DeadTCR					DEADTBE	DEADTAE	DEADTP1	DEADTP0
							R/W	R/W	R/W	R/W
Bank 1	0x15	DeadTR					DEADTR3	DEADTR2	DEADTR1	DEADTR0
							R/W	R/W	R/W	R/W
Bank 1	0x16	PWMSCR				DEADS			PWMBS	PWMAS
						R/W			R/W	R/W
Bank 1	0x17	PWMACR	PWMAE	IPWMAE	PWMAA	IPWMAA	TAEN	TAP2	TAP1	TAP0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x18	PRDAL	PRDA7	PRDA6	PRDA5	PRDA4	PRDA3	PRDA2	PRDA1	PRDA0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x19	PRDAH							PRDA9	PRDA8
									R/W	R/W
Bank 1	0x1A	DTAL	DTA7	DTA6	DTA5	DTA4	DTA3	DTA2	DTA1	DTA0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x1B	DTAH							DTA9	DTA8
									R/W	R/W
Bank 1	0x1C	TMRAL	TMRA7	TMRA6	TMRA5	TMRA4	TMRA3	TMRA2	TMRA1	TMRA0
			R	R	R	R	R	R	R	R
Bank 1	0x1D	TMRAH							TMRA9	TMRA8
									R	R
Bank 1	0x1E	PWMBCR	PWMBE	IPWMBE	PWMBA	IPWMBA	TBEN	TBP2	TBP1	TBP0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x1F	PRDBL	PRDB7	PRDB6	PRDB5	PRDB4	PRDB3	PRDB2	PRDB1	PRDB0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x20	PRDBH							PRDB9	PRDB8
									R/W	R/W
Bank 1	0x21	DTBL	DTB7	DTB6	DTB5	DTB4	DTB3	DTB2	DTB1	DTB0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x22	DTBH							DTB9	DTB8
									R/W	R/W
Bank 1	0x23	TMRBL	TMRB7	TMRB6	TMRB5	TMRB4	TMRB3	TMRB2	TMRB1	TMRB0
			R	R	R	R	R	R	R	R
Bank 1	0x24	TMRBH							TMRB9	TMRB8
									R	R

6.8.1 Overview

In PWM mode, it produces up to 10-bit resolution PWM output (see Functional Block Diagram). A PWM output consists of a time period and a duty cycle, and it keeps the output high. The baud rate of the PWM is the inverse of the time period. Figure 25~28 (*PWM Output Timing*) depict the relationships between a time period and a duty cycle.

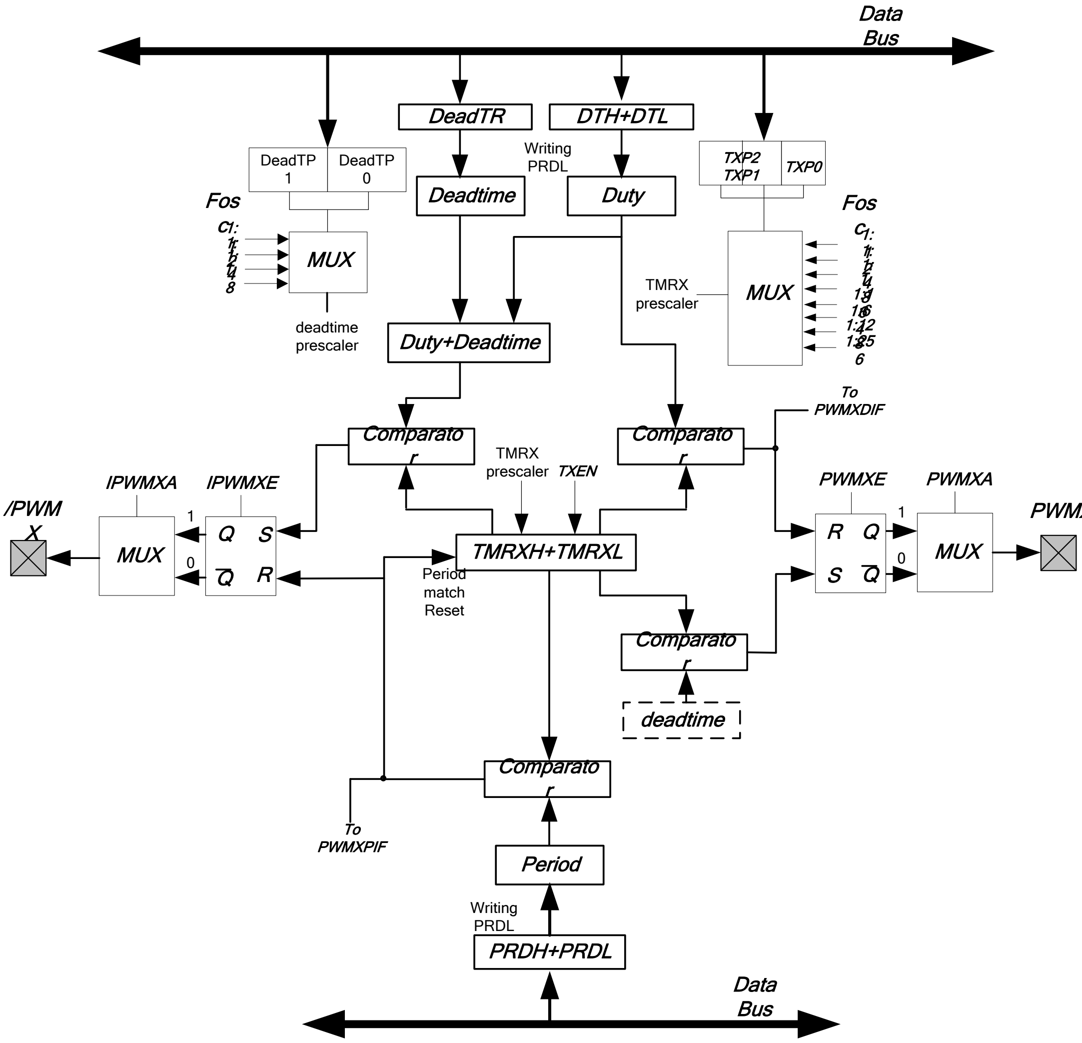


Figure 2. The PWM Functional Block Diagram

PWM and /PWM (inverted PWM) can be used individually or used as dual PWM. When used individually, the definitions of active level between PWM and /PWM are somewhat different.

For example, set period and duty cycle (period > duty), PWMXE=1/0 and IPWMXE=0/1, PWMXA = 1/0, IPWMXA=1/0, and finally set TXEN = 1. The following figures show PWM output timing according to different PWMXA and IPWMXA settings.

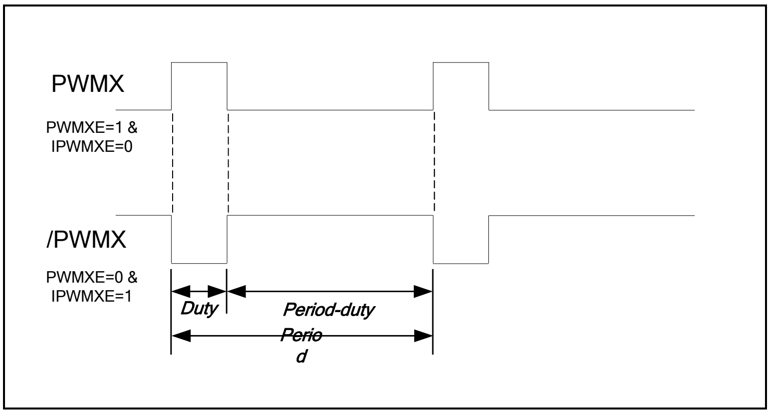


Figure 3.PWM Output Timing (PWMXA=0 and IPWMXA=0)

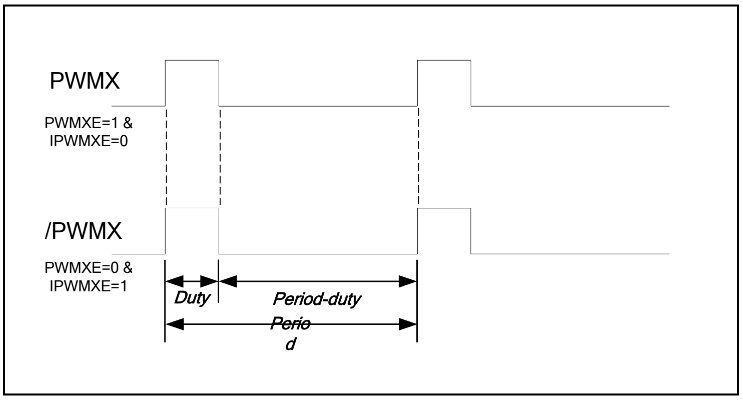


Figure 4.PWM Output Timing (PWMXA=0 and IPWMXA=1)

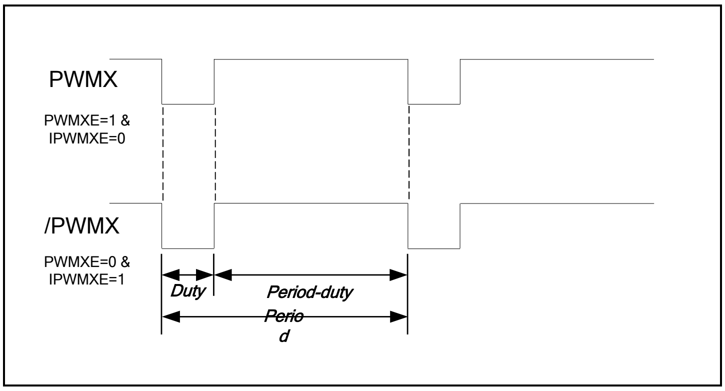


Figure 5.PWM Output Timing (PWMXA=1 and IPWMXA=0)

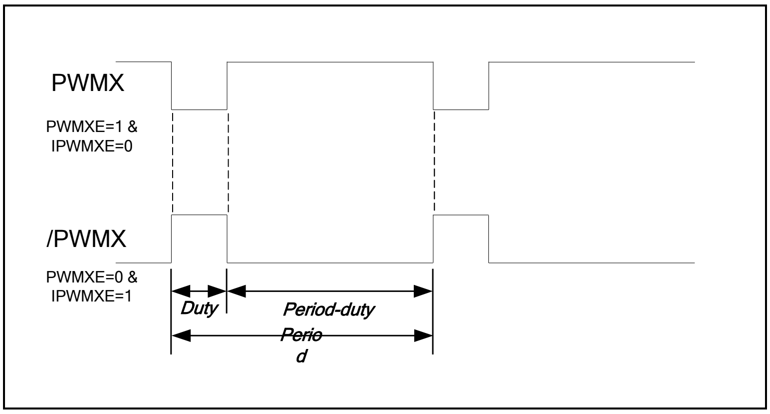


Figure 6.PWM Output Timing (PWMXA=1 and IPWMXA=1)

For the shut-off of the operating PWM function, refer to Figure 31.

6.8.2 Increment Timer Counter (TMRX: TMRAH/TMRAL or TMRBH/TMRBL)

TMRX are 10-bit clock counters with programmable prescaler. They are designed for the PWM module as baud rate clock generators. TMR can be read-only. If employed, they can be turned off for power saving by setting the TAEN bit [BANK1-R1A <3>], TBEN bit [BANK1-R21<3>].

TMRA, and TMRB are internal designs and cannot be set.

6.8.3 PWM Time Period (PRDX: PRDAL/H or PRDBL/H)

The PWM period is 10-bit resolution. The PWM time period is defined by writing to the PRDX register. When TMRX is equal to PRDX, the following events occur on the next increment cycle**:**

- TMRX is cleared
- The PWMX pin is set to 1

> **NOTE**
> *The PWM output will not be set, if the duty cycle is 0*

- The PWMXIF pin is set to 1

The following formula describes how to calculate the PWM time period**:**

$$Period = (PRDX + 1) \times \left(\frac{1}{F_{OSC}}\right) \times \frac{CLKS}{2} \times (TMRX\ \ prescale\ value)$$

Example:

PRDX = 49; Fosc = 4 MHz; TMRX (0, 0, 0) = 1 : 1,

CLKS bit of the Code Option Register = 0 (two oscillator periods);

Then

$$Period = (49 + 1) \times \left(\frac{1}{4M}\right) \times \frac{2}{2} \times 1 = 12.5\mu s$$

6.8.4 PWM Duty Cycle (DTX: DTAH/DTAL or DTBH/DTBL)

The PWM duty cycle is defined by writing to the DTX register, and is latched from DTX to DLX while TMRX is cleared. When DLX is equal to TMRX, the PWMX pin is cleared. DTX can be loaded anytime. However, it cannot be latched into DLX until the current value of DLX is equal to TMRX.

The following formula describes how to calculate the PWM duty cycle**:**

$$Duty\ cycle\ = (DTX) \times \left(\frac{1}{F_{OSC}}\right) \times \frac{CLKS}{2} \times (TMRX\ \ prescale\ value)$$

Example:

DTX = 10;   Fosc = 4 MHz;   TMRX (0, 0, 0) = 1 : 1,

CLKS bit of the Code Option Register = 0 (two oscillator periods);

Then

$$Duty\ cycle\ = (10) \times \left(\frac{1}{4M}\right) \times \frac{2}{2} \times 1 = 2.5\mu s$$

6.8.5 Dual PWM function

It consists of a complementary PWM (i.e. PWMX and /PWMX), one outputs PWM signal and one outputs inverted PWM signal, which outputs any pulse width signal user wish by programming relative control registers.

The dead time mode is supported. It means that the complementary PWM signals can be controlled to get a time interval that the complementary PWM signals won't be intersected.

The following Figures 7 ~ 9 show the dual PWM output waveform.

Disable dead time control (DEADTXE = 0). Set period and duty cycle (period > duty). Set PWMXE & IPWMXE =1, PWMXA = 0/1, IPWMXA = 0/1, and finally set TXEN = 1.

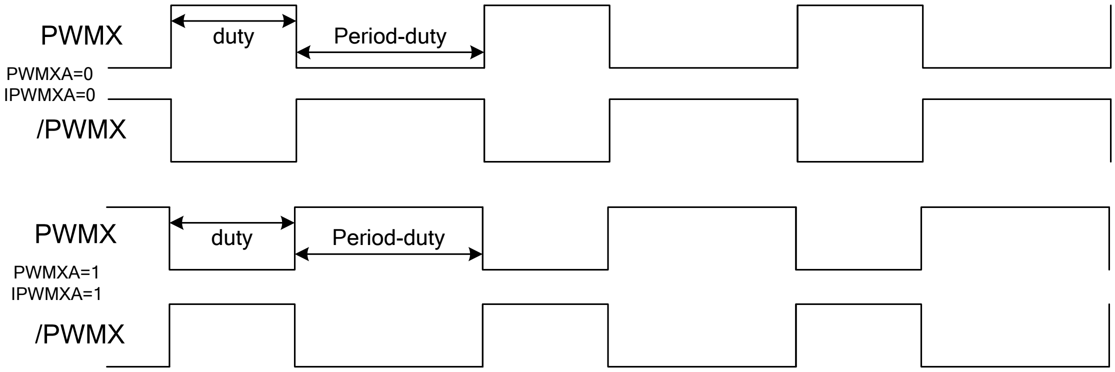


Figure 7. Dual PWMX output waveform (DEADTXE = 0)

Set dead time > 0 (set dead time prescaler if required). Enable dead time control (DEADTXE = 1). Set period and duty cycle (period > duty). Set PWMXE & IPWMXE =1, PWMXA = 0, IPWMXA = 0, and finally set TXEN = 1. For the loading new duty, period, and dead time value at run time, refer to subchapter *PWM Programming Process/Steps*.

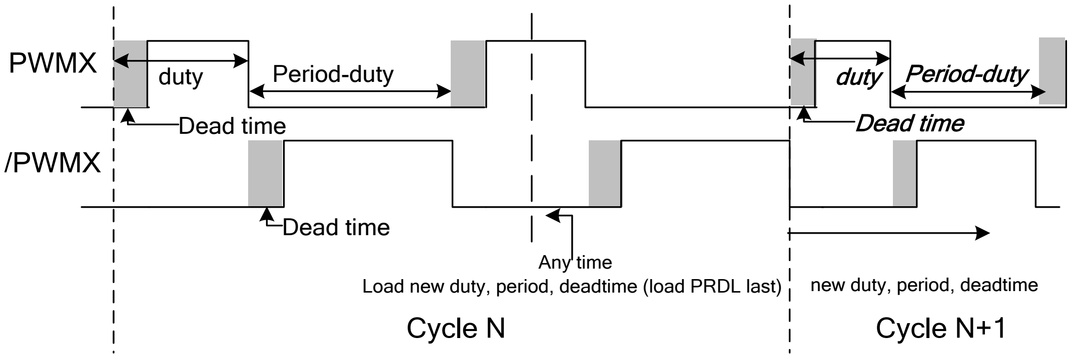


Figure 8. Dual PWMX output waveform (DEADTXE = 1, Dead Time > 0)

User can make use of the falling edge of comparator's output to close dual PWM or single PWM function by setting SDPWMX=1. The following figure shows how to shut down a dual PWM.

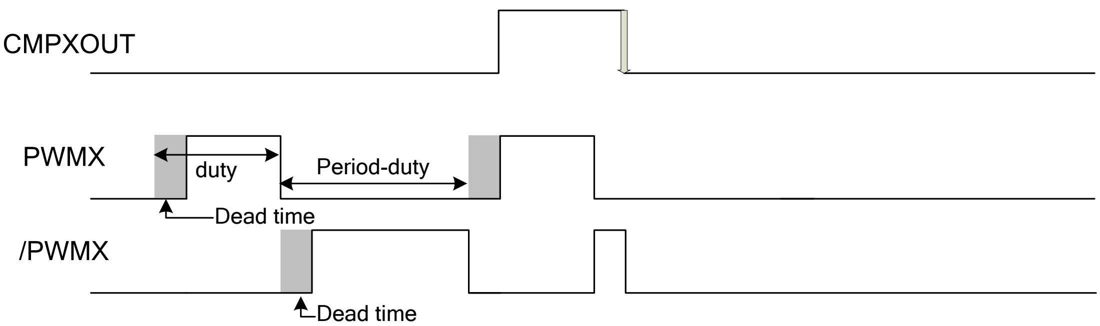


Figure 9. Dual PWMX output waveform (DEADTXE = 1, Dead Time ≧ 0, SDPWMX = 1)

6.8.6 Comparator

Changing the output status while matching occurs will simultaneously set the TMRXIF flag.

6.8.7 PWM Programming Process/Steps

1. Load the PWM duty cycle to DT.
2. Load the PWM dead-time cycle (only for dual PWM function).
3. Load the PWM time period to PRD.
4. Enable the interrupt function by writing Bank0-R1D, if required.
5. Load a desired value for the timer prescaler.
6. Set active level of duty of PWM.
7. Enable PWMX function, i.e., enable PWMXE control bit. (If using dual PWM function, enable IPWMXE control bit too)
8. Finally, enable TMRX function, i.e., enable TXEN control bit.

If the application needs to change PWM duty, period, and dead-time cycle at run time, refer to the following programming steps:

1. Load new duty and dead-time cycle (if using dual PWM function) at any time.
2. Load new period cycle. The order of loading period cycle must be taken care. **As the low byte of PWM period cycle is assigned a value, the new PWM cycle is loaded into circuit**.
3. The circuit would automatically update the new duty, period, and dead-time cycle to generate new PWM waveform at the next PWM cycle.

6.9 Comparator

R_BANK	Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 0	0x10	WUCR1		CMPWK						
				R/W						
Bank 0	0x14	SFR1		CMPSF						
				R/W						
Bank 0	0x1B	IMR1		CMPIE						
				R/W						
Bank 0	0x3A	CMPCR1	CRS	CPOUT	CS1	CS0		CC+S1	CC+S0	SDPWMA
			R/W	R/W	R/W	R/W			R/W	R/W
Bank 0	0x3B	CMPCR2							CIRL2	SDPWMB
									R/W	R/W
Bank 0	0x3C	CMPCR3						CIRL1	CIRL0	
								R/W	R/W	

The MCU has four comparators comprising of two analog inputs and one output. All of comparators can be as OP. The comparator can be utilized to wake up the MCU from sleep mode. The comparator circuit diagram is depicted in the figure below.

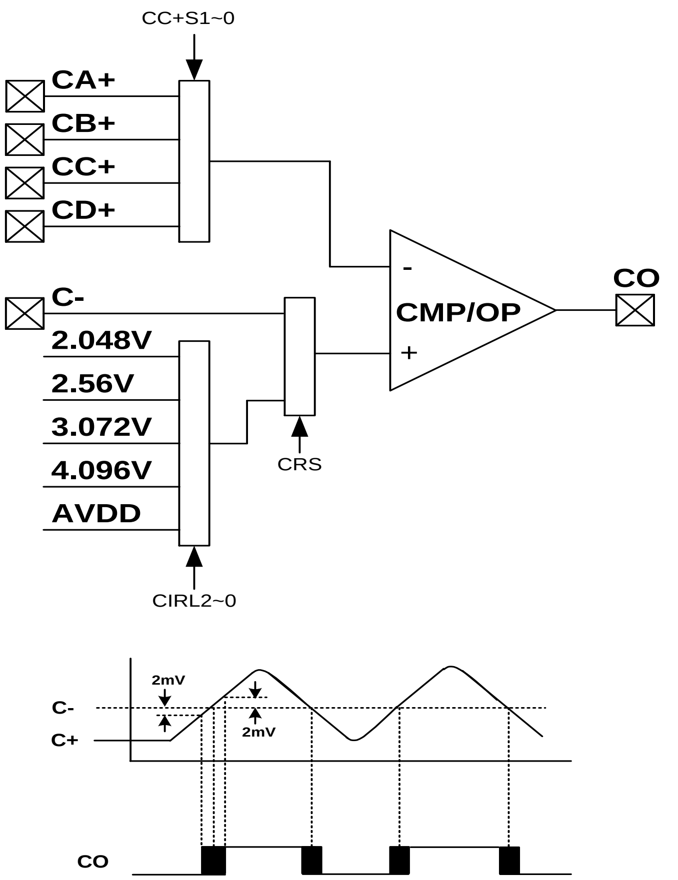


Figure 10. Comparator Circuit Diagram & Operating Mode

6.9.1External Reference Signal

The analog signal that is presented at Cin– compares to the signal at Cin+, and the digital output (CO) of the comparator is adjusted accordingly by taking the following notes into considerations**:**

> ***NOTE***
>
> - *The reference signal must be between Vss and Vdd.*
> - *Comparator with function of internal reference and corresponding pin can be set as comparator I/O or general I/O.*
> - *The non-inverting end of comparator can be connected to Vref.*
> - *The three reference voltage levels for Vref are of 2.048V 2.56, 3.072V and 4.096V.*
> - *The falling edge of CO can turn off the corresponding only PWMx or both of PWMx and /PWMx, depends on the PWMxA and IPWMXA. For example,*
>
> *(falling edge of CO ≥ PWMA or both of PWMA and /PWMA)*

6.9.2Comparator Outputs

- The compared result is stored in the CMPOUT.
- The pin (CO) function is decided through programming the register <CS[1:0]>.

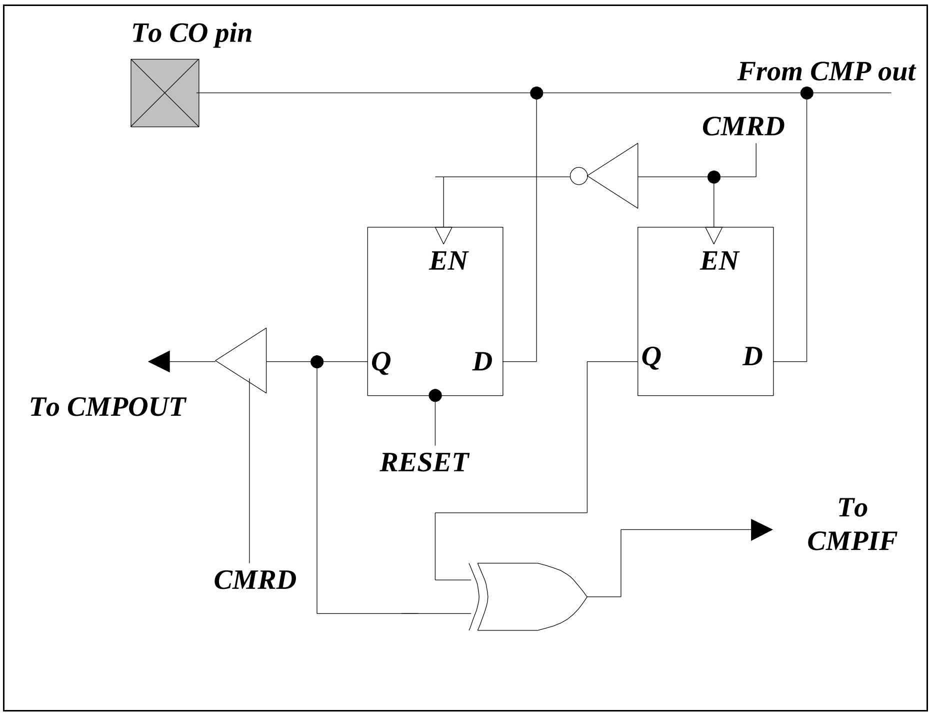


Figure 11. Comparator Output Configuration

6.9.3Comparator Interrupt

- CMPXIE must be enabled for the “ENI” instruction to take effect
- Interrupt is triggered whenever a change occurs on the comparator output pin
- The actual change on the pin can be determined by reading the Bit CPXOUT
- The comparator interrupt flag, CMPXIF, can only be cleared by software

6.9.4Wake-up from SLEEP Mode

- The comparator and the interrupt remains active in SLEEP mode when CMPXIE=1 and CMPWK=1.
- If a comparator output changes state, the interrupt will wake up the device from SLEEP mode.
- The power consumption should be taken into consideration for the benefit of energy conservation.
- If the function is unemployed during SLEEP mode, turn off comparator before entering into sleep mode.

6.10 UART (Universal Asynchronous Receiver/Transmitter)

Registers for UART Circuit

R_BAN	Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 0	0x16	SFR2	-	-	UERRSF	URSF	UTSF	-	-	-
			-	-	R/W	R/W	R/W	-	-	-
Bank 0	0x1C	IMR2	-	-	UERRIE	URIE	UTIE	-	-	-
			-	-	R/W	R/W	R/W	-	-	-
Bank 1	0X33	URCR	UINVEN	UMODE1	UMODE0	BRATE2	BRATE1	BRATE0	UTBE	TXE
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0X34	URS	URTD8	EVEN	PRE	PRERR	OVERR	FMERR	URB	RXE
			W	R/W	R/W	R/W	R/W	R/W	R	R/W
Bank 1	0x35	URTD	URTD7	URTD6	URTD5	URTD4	URTD3	URTD2	URT	URT
			W	W	W	W	W	W	W	W
Bank 1	0X36	URRDL	URRD7	URRD6	URRD5	URRD4	URRD3	URRD2	URR	URR
			R	R	R	R	R	R	R	R
Bank 1	0X37	URRDH	URRD8	-	-	-	-	-	-	-
			R	-	-	-	-	-	-	-

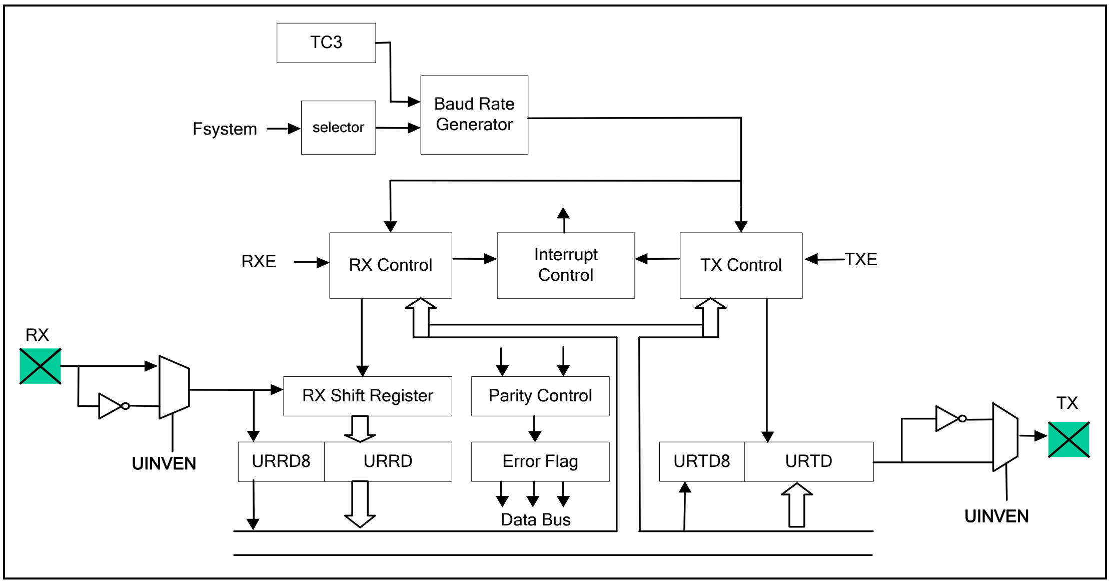


Figure 6-16 UART Functional Block Diagram

In Universal Asynchronous Receiver Transmitter (UART), each transmitted or received character is individually synchronized by framing it with a start bit and stop bit.

Full duplex data transfer is possible since the UART has independent transmit and receive sections. Double buffering for both sections allows the UART to be programmed for continuous data transfer.

The figure below shows the general format of one character sent or received. The communication channel is normally held in the marked state (high). Character transmission or reception starts with a transition to the space state (low).

The first bit transmitted or received is the start bit (low). It is followed by the data bits, in which the least significant bit (LSB) comes first. The data bits are followed by the parity bit. If present, then the stop bit or bits (high) confirms the end of the frame.

In receiving, the UART synchronizes on a falling edge of the start bit. When two or three “0” are detected during three samples, it is recognized as normal start bit and the receiving operation is started.

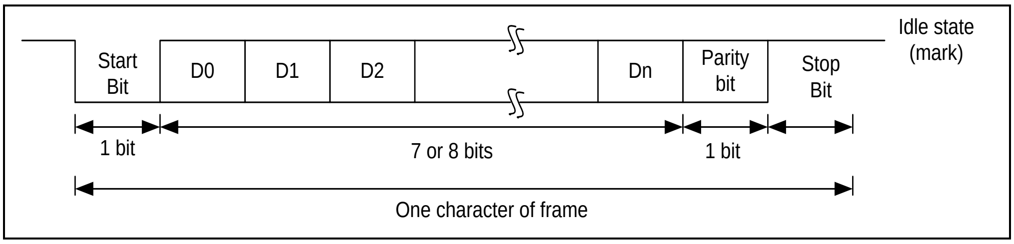


Figure 6-17 Data Format in UART

6.10.1 UART Mode

There are three UART modes. Mode 1 (7 bits data) and Mode 2 (8 bits data) allow the addition of a parity bit. The parity bit addition is not available in Mode 3. Figure 6-18a below shows the data format in each mode.

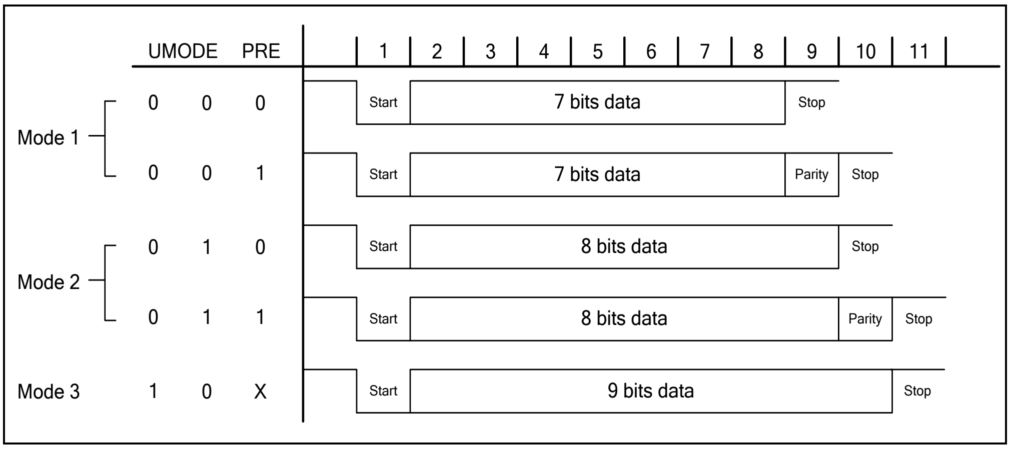


Figure 6-18a UART Model

6.10.2 Transmitting

In transmitting serial data, the UART operates as follows:

1. Set the TXE bit of the URCR1 register to enable the UART transmission function.
2. Write data into the URTD register and the UTBE bit of the URCR register will be cleared by hardware.
3. Then start transmitting.
4. Serially transmitted data are transmitted in the following order from the TX pin.
5. Start bit: one “**0**” bit is output.
6. Transmit data: 7, 8 or 9 bits data are output from the LSB to the MSB.

7. Parity bit: one parity bit (odd or even selectable) is output.
8. Stop bit: one "**1**" bit (stop bit) is output.

Mark state: output "1" continues until the start bit of the next transmitted data.

After transmitting the stop bit, the UART generates a UTSF interrupt (if enabled).

6.10.3 Receiving

In receiving, the UART operates as follows:

1. Set the RXE bit of the URS register to enable the UART receiving function. The UART monitors the RX pin and synchronizes internally when it detects a start bit.
2. Received data is shifted into the URRD register in the order from LSB to MSB.
3. The parity bit and the stop bit are received. After one character is received, the URBF bit of the URS register will be set to "**1**". This means UART interrupt will occur.
4. The UART makes the following checks:
   (a) Parity check: The received data with number of "1" must match the even or odd parity setting of the EVEN bit in the URS register.
   (b) Frame check: The start bit must be "0" and the stop bit must be "1".
   (c) Overrun check: The URBF bit of the URS register must be cleared (that means the URRD register should be read out) before the next received data is loaded into the URRD register.

   If any checks failed, the UERRSF interrupt will be generated (if enabled), and an error flag is indicated in PRERR, OVERR or FMERR bit. The error flag should be cleared by software, otherwise, UERRSF interrupt will occur when the next byte is received.
5. Read received data from URRD register. And URBF bit will be set by hardware.

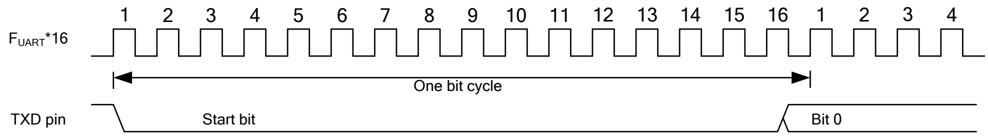
6.10.4 Baud Rate Generator

The baud rate generator is comprised of a circuit that generates a clock pulse to determine the transfer speed for transmission/reception in the UART.

The BRATE2~BRATE0 bits of the URC register can determine the desired baud rate.

6.10.5 UART Timing

1. Transmission Counter Timing:



2. Receiving Counter Timing:

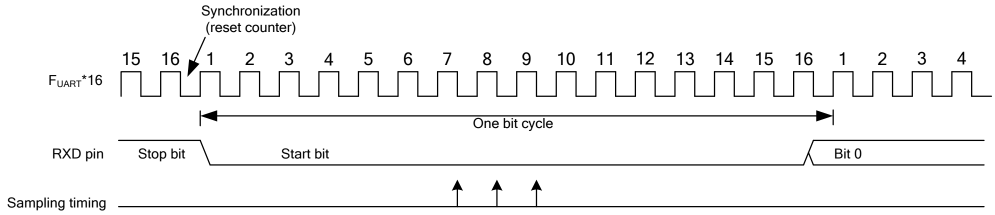


Figure 6-18b UART Timing Diagrams

6.11 SPI (Serial Peripheral Interface)

R_BANK	Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 0	0X36	SPICR	CES	SPIE	SRO	SSE	SDOC	SBRS2	SBRS1	SBRS0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0X37	SPIS	DORD	TD1	TD0	-	OD3	OD4	-	RBF
			R/W	R/W	R/W	-	R/W	R/W	-	R
Bank 0	0X38	SPIR	SRB7	SRB6	SRB5	SRB4	SRB3	SRB2	SRB1	SRB0
			R	R	R	R	R	R	R	R
Bank 0	0X39	SPIW	SWB7	SWB6	SWB5	SWB4	SWB3	SWB2	SWB1	SWB0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0X18	SFR4	-	-	-	-	SPISF	-	-	-
			-	-	-	-	R/W	-	-	-
Bank 0	0X1E	IMR4	-	-	-	-	SPIIE	-	-	-
			-	-	-	-	R/W	-	-	-

6.11.1 Overview and Feature

Overview:

Figures 6-19 and 6-20 show how EM88F712N communicates with other devices through SPI module. If EM88F712N is a Master controller, it sends clock through the SCK pin. A couple of 8-bit data are transmitted and received at the same time. However, if EM88F712N is defined as a Slave, its SCK pin could be programmed as an input pin. Data will continue to be shifted based on both clock rate and selected edge. User can also set SPIS Bit 7 (DORD) to determine SPI transmission order; set SPICR Bit 3 (SDOC) to control SDO pin after serial data output status; and set SPIS Bit 6 (TD1) and Bit 5 (TD0) to determine the SDO status output delay times.

Features:

1. Operation in either Master mode or Slave mode
2. Three-wire or four-wire full duplex synchronous communication
3. Programmable baud rates of communication
4. Programming clock polarity, (Bank 0 R36 Bit 7)
5. Interrupt flag available for the read buffer full
6. SPI transmission order
7. After serial data output SDO status select
8. SDO status output delay times
9. SPI handshake pin
10. Up to 4 MHz (maximum) bit frequency

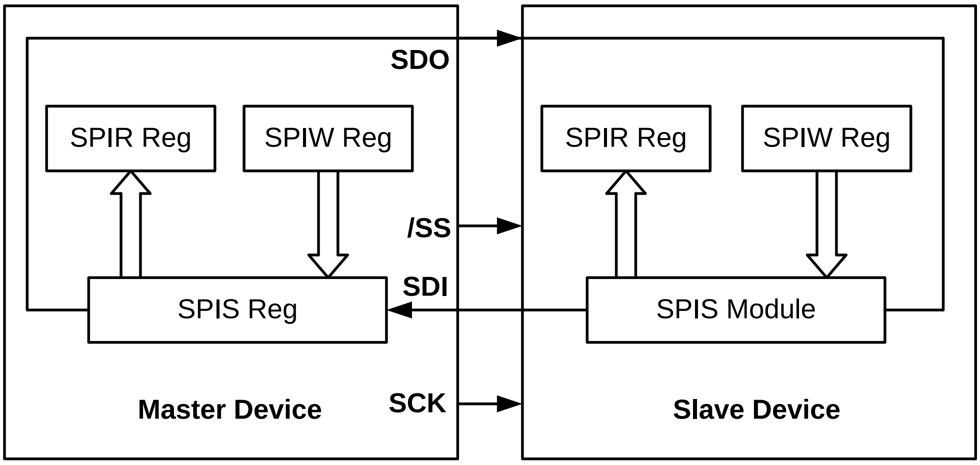


Figure 6-19 SPI Master/Slave Communication

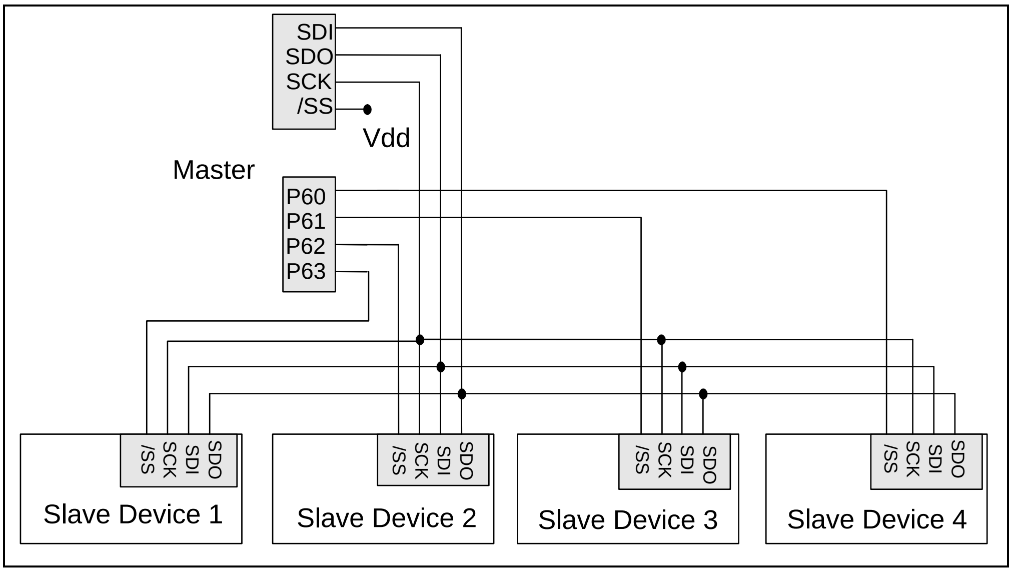


Figure 6-20 SPI Configuration of Single-Master and Multi-Slave

6.11.2 SPI Functional Description

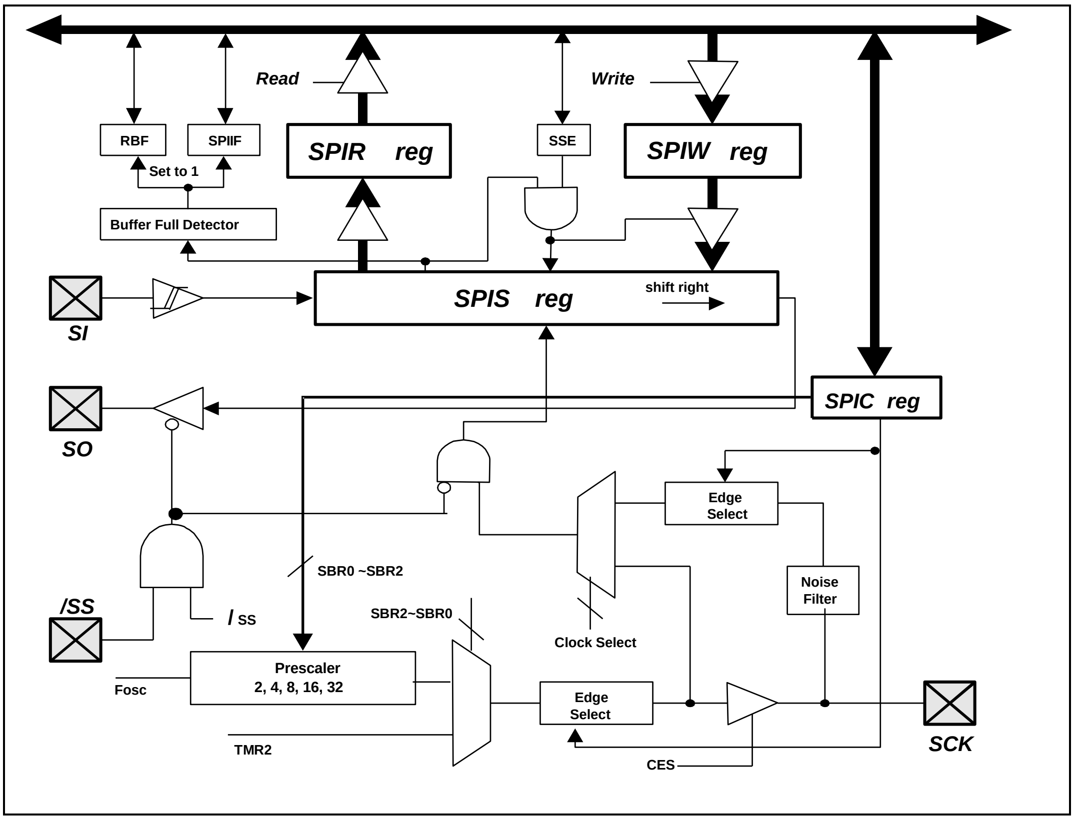


Figure 6-21 SPI Block Diagram

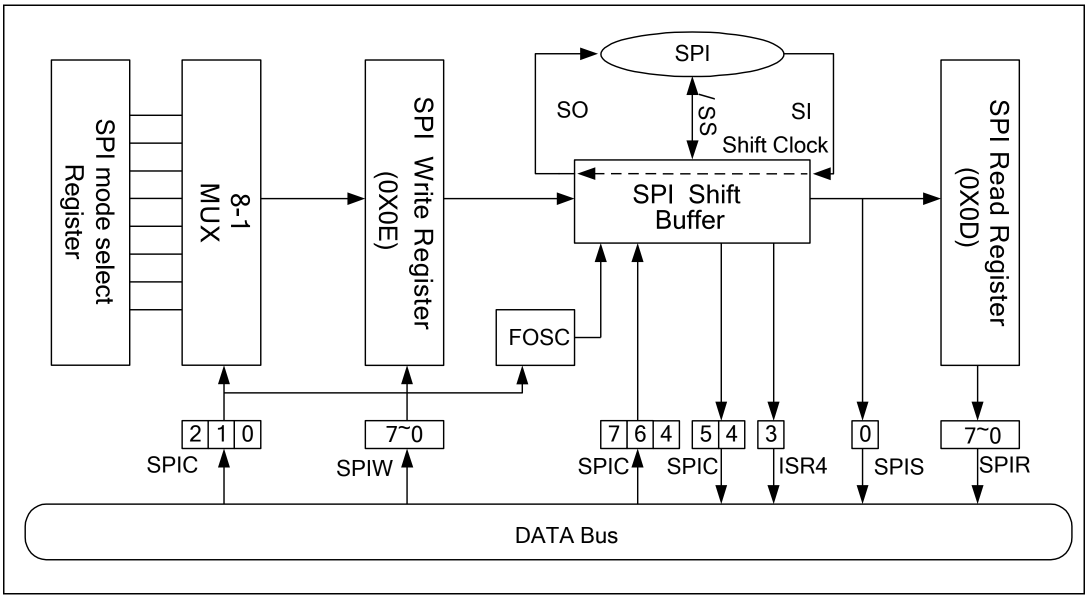


Figure 6-22 Functional Block Diagram of SPI Transmission

Below are the functions of each block and explanations on how to carry out the SPI communication with the signals depicted in Figures 6-21 and 6-22.

- P84/SDA/SI/SEG4: Serial Data In
- P85/SO/SEG5: Serial Data Out
- P86/SCL/SCK/SEG6: Serial Clock
- P87//SS/AD9/SEG8: /Slave Select (Option). This pin (/SS) may be required during Slave mode
- RBF: Set by Buffer Full Detector
- Buffer Full Detector: Set to 1 when an 8-bit shifting is completed.
- SSE: Load the data in SPIS register, and begin shifting.
- SPIS reg.: Shifting byte in and out. The MSB is shifted first. Both the SPIR and the SPIW registers are shifted at the same time. Once data are written, SPIS starts transmission / reception. The received data will be moved to the SPIR register as the shifting of the 8-bit data is completed. The RBF (Read Buffer Full) flag and the SPISF (SPI Interrupt) flag are then set.
- SPIR reg.: Read buffer. The buffer will be updated as the 8-bit shifting is completed. The data must be read before the next reception is completed. The RBF flag is cleared as the SPIR register reads.
- SPIW reg.: Write buffer. The buffer will deny any attempts to write until the 8-bit shifting is completed.

The SSE bit will be kept in “1” if the communication is still undergoing. This flag must be cleared as the shifting is completed. Users can determine if the next write attempt is available.

- SBRS2~SBRS0: Programming the clock frequency/rates and sources.
- Clock Select: Selecting either the internal or the external clock as the shifting clock.
- Edge Select: Selecting the appropriate clock edges by programming the CES bit

6.11.3 SPI Signal and Pin Description

The detailed functions of the four pins, SI, SO, SCK, and /SS are as follows:

P84/SDA/SI/SEG4:

- Serial Data In
- Receive sequentially, the Most Significant Bit (MSB) first, Least Significant Bit (LSB) last,
- Defined as high-impedance, if not selected

- Program the same clock rate and clock edge to latch on both the Master and Slave devices
- The received byte will update the transmitted byte
- The RBF will be set as the SPI operation is completed
- Timing is shown in Figures 6-23 and 6-24.

P85/SO/SEG5:

- Serial Data Out
- Transmit sequentially; Most Significant Bit (MSB) first, Least Significant Bit (LSB) last
- Program the same clock rate and clock edge to latch on both the Master and Slave devices
- The received byte will update the transmitted byte
- CES bit will be reset, as the SPI operation is completed
- Timing is shown in Figures 6-23 and 6-24.

P86/SCL/SCK/SEG6:

- Serial Clock
- Generated by a Master device
- Synchronize the data communication on both SI and SO pins
- CES is used to select the edge to communicate.
- SBR0~SBR2 are used to determine the baud rate of communication
- CES, SBR0, SBR1, and SBR2 bits have no effect in Slave mode
- Timing is shown in Figures 6-23 and 6-24.

P87//SS/AD9/SEG8:

- Slave Select; negative logic
- Generated by a Master device to signify the Slave(s) to receive data
- Go low before the first cycle of SCK appears, and remains low until the last (eighth) cycle is completed
- Ignore the data on the SI and SO pins while /SS is high, because the SO is no longer driven
- Timing is shown in Figures 6-23 and 6-24.

6.11.4 SPI Mode Timing

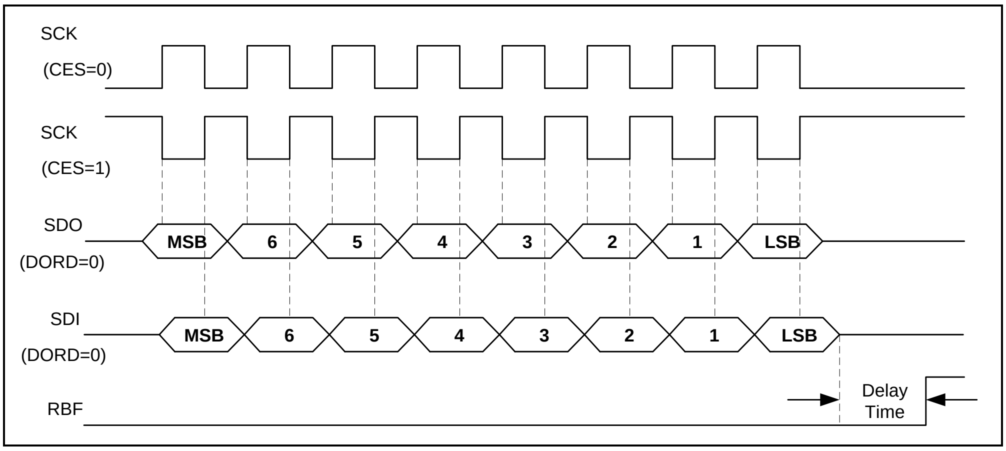


Figure 6-23 SPI Mode with /SS Disabled

The SCK edge is selected by programming bit CES. The waveform shown in Figure 6-23 is applicable regardless of whether the EM88F712N is in Master or Slave mode, with /SS disabled. However, the waveform in Figure 6-24 can only be implemented in Slave mode with /SS enabled.

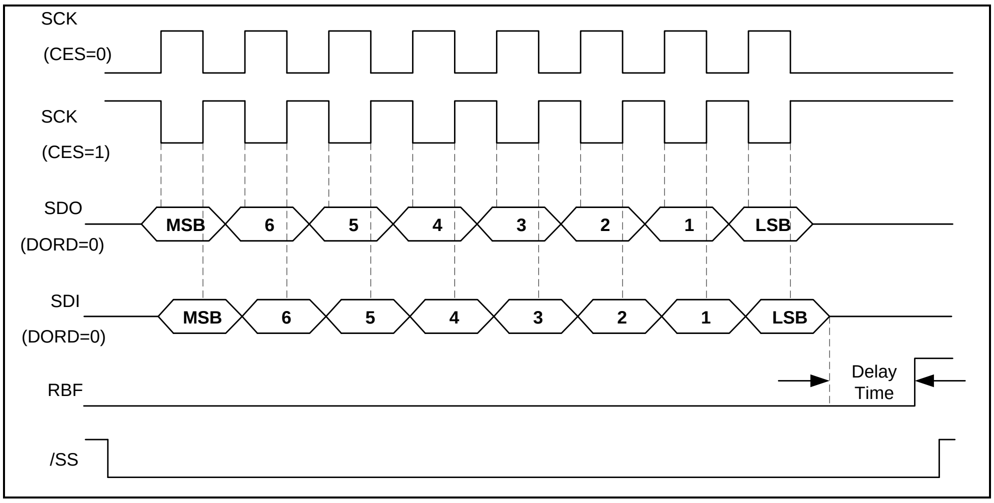


Figure 6-24 SPI Mode with /SS Enabled

6.12 HLVD (High / Low Voltage Detector)

R_BANK	Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit0
Bank 1	**0x49**	**HLVDCR**	HLVDEN	IRVSF	VDSB	VDM	HLVDS3	HLVDS2	HLVDS1	HLVDS0
			R/W	R	R	R/W	R/W	R/W	R/W	R/W
Bank 0	**0x14**	**SFR**			HLVDSF					
					R/W					
Bank 0	**0x1B**	**IMR**			HLVDIE					
					R/W					
Bank 0	**0x10**	**WUCR**			HLVDWK					
					R/W					

Under unstable power source condition, such as external power noise interference or EMS test condition, a violent power vibration could occur. At the time, the VDD could become unstable as it could be operating below working voltage. When the system supply voltage (VDD) falls below operating voltage, the IC kernel will automatically keep all register statuses.

The following steps are needed to setup HLVD function:

1. Set HLVDEN to “1”, then use Bits 3~0 (HLVDS3~HLVDS0) of Register Bank 1 R49 to set the HLVD interrupt level
2. Wait for HLVD interrupt to occur
3. Clear HLVD interrupt flag

The internal HLVD module uses the internal circuit to fit. When user set HLVDEN to enable the HLVD module, the current consumption will increase to 70 µA.

During sleep mode, HLVD module continues to operate. If the device voltage drops slowly and crosses the detect point, HLVDSF bit will be set and the device will not wake up from Sleep mode. Until another wake-up source wakes up EM88F712N, HLVD interrupt flag will remain as the prior status.

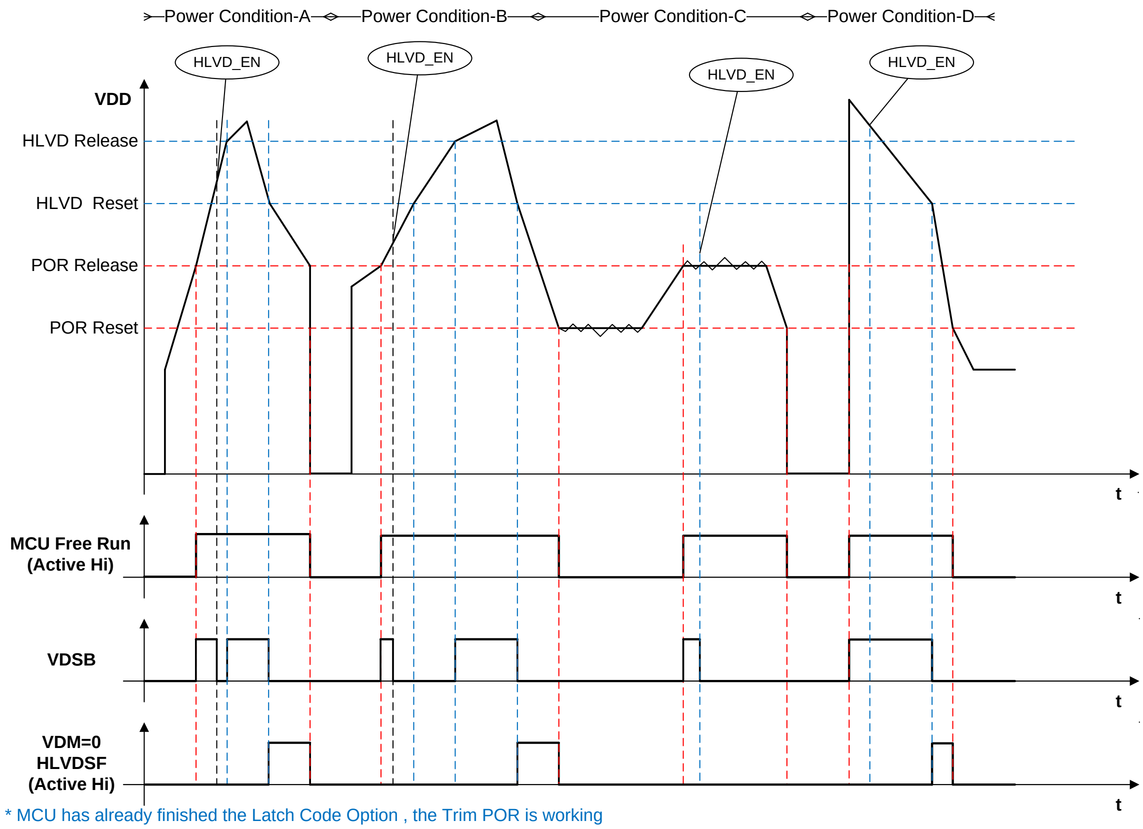
When the system resets, the HLVD flag will be cleared.

The Figure 6-30 illustrates HLVD module detecting an external voltage.

When VDD drops yet not below V_{LVD}, HLVDSF remains at “0”.

When VDD drops below VDB, HLVDSF is set to “1”. If global ENI is enabled, HLVDSF will be set to “1” as well, and the next instruction will branch to the interrupt vector. The HLVD interrupt flag is cleared to “0” by software.

When VDD drops below V_{RESET} is less than 10 µs, the system will keep all the register statuses and the system halts but oscillation is active. When VDD drops below V_{RESET} and more for than 40 µs, system RESET will occur. Refer to Section 6.5.1 *Reset description.*



* MCU has already finished the Latch Code Option , the Trim POR is working
* Trim POR has 1us deglitch , response time us @ over drive mV

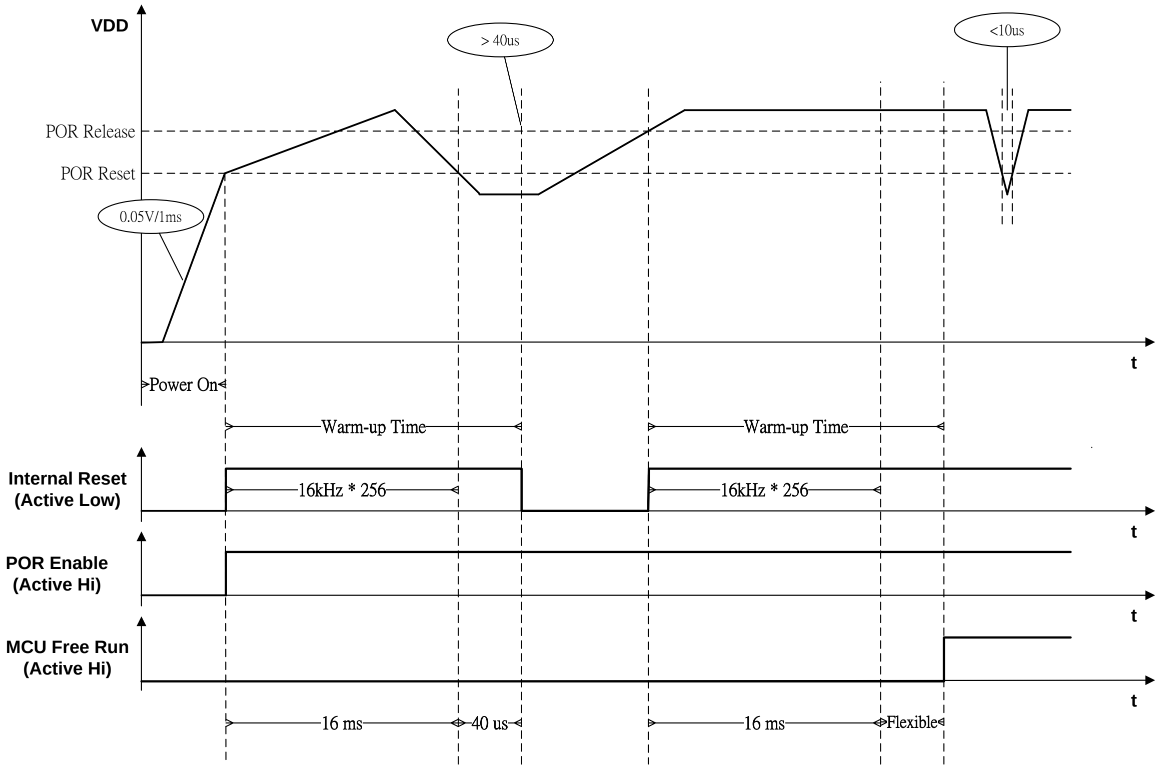


Figure 6-30 HLVD Waveform Characteristics Showing Detection Point in an External Voltage Condition

6.13 Oscillator

6.13.1Oscillator Modes

The EM88F712N can be operated in two different oscillator modes, such as Internal RC oscillator mode (IRC) and XTAL oscillator mode (XT). User need to set the main-oscillator modes by selecting the OSC2~OSC0, and set the sub-oscillator modes by selecting the FSS0 in the Code Option register to complete the overall oscillator mode setting. Tables 6, 7, and 8 depict how these four modes are defined.

The up-limited operating frequency of crystal/resonator on the different VDD is listed in Table 6.

Table 6 Main-oscillator modes defined by OSC2 ~ OSC0

Main-oscillator Mode	OSC2	OSC1	OSC0
IRC (Internal RC oscillator mode) (default) RCOUT (P51) acts as I/O pin	0	0	0
IRC (Internal RC oscillator mode) RCOUT (P51) acts as clock output pin	0	0	1
HXT1 (High XTAL1 oscillator mode) Frequency range: 12~20MHz	0	1	0
HXT2(High XTAL2 oscillator mode) Frequency range: 6~12MHz	0	1	1
XT (XTAL oscillator mode) Frequency range: 1~6MHz	1	0	0
LXT1 (Low XTAL1 oscillator mode) Frequency range: 100K~1MHz	1	0	1
Reserve	1	1	X

Table 9 Summary of Maximum Operating Speeds

Conditions	VDD	Fxt max. (MHz)
Two cycles with two clocks	2.2	8.0
	3.3	16.0
	5.0	20.0

6.13.2 Crystal Oscillator/Ceramic Resonators (XTAL)

In most applications, Pin OSCI and Pin OSCO can be connected with a crystal or ceramic resonator to generate oscillation and such circuitry are depicted in the following figures. The same thing applies whether it is in HXT or LXT mode. Table 10 provides the recommended values of C1 and C2. Since each resonator has its own attribute, user should refer to its specification for appropriate values of C1 and C2. The serial resistor, RS, may be necessary for AT strip cut crystal in low frequency mode.

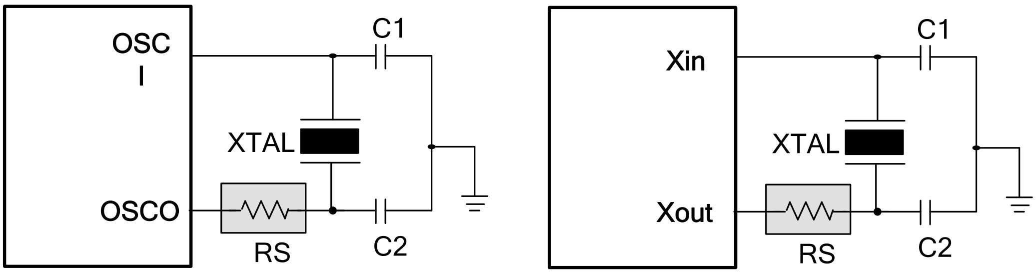


Figure 6-31 Crystal/Resonator Circuits

Table 10 Capacitor Selection Guide for Crystal Oscillator or Ceramic Resonator

Oscillator Type	Frequency Mode	Frequency	C1 (pF)	C2 (pF)
Main-oscillator (Ceramic Resonators)	LXT (100K~1 MHz)	100kHz	60pF	60pF
		200kHz	60pF	60pF
		455kHz	40pF	40pF
		1.0 MHz	30pF	30pF
	HXT2 (1M~6 MHz)	1.0 MHz	30pF	0pF
		2.0 MHz	30pF	30pF
		4.0 MHz	20pF	20pF
Main-oscillator (Crystal Oscillator)	LXT (100K~1 MHz)	100kHz	60pF	60pF
		200kHz	60pF	60pF
		455kHz	40pF	40pF
		1.0 MHz	30pF	30pF
	XT (1M~6 MHz)	1.0 MHz	30pF	30pF
		2.0 MHz	30pF	30pF
		4.0 MHz	20pF	20pF
		6.0 MH	0F	30pF
	HXT2 (6M~12 MHz)	6.0 MHz	30pF	30pF
		8.0 MHz	20pF	20pF
		12.0 MHz	30pF	30pF
	HX1 (12M~16 MHz)	12.0 MHz	30pF	30pF
		16.0 MHz	20pF	20pF

6.13.3 Internal RC Oscillator Mode

EM88F712N offer a versatile internal RC mode with default frequency value of 4MHz. The Internal RC oscillator mode has other frequencies (20MHz, 16MHz, 12MHz, 10MHz, 8MHz, 4MHz and 1 MHz) that can be set by Code Options RCM1 and RCM0. All these four main frequencies can be calibrated by programming the Code Option bits: C6~C0. The table below describes a typical instance of the calibration.

Internal RC Drift Rate (Ta=25°C, VDD=5V, VSS=0V, IRCPSS =0)

Internal RC Frequency	Drift Rate= Temperature (-40℃~+85℃)+ Voltage (2.2V~5.5V) (IRCPSS =0) + Process	
	NUWTR Total	UWTR Total
1MHz	±4%	±5%
4MHz	±4%	±5%
8MHz	±4%	±5%
10MHz	±4%	±5%
12MHz	±4%	±5%
16MHz	±4%	±5%
20MHz	±4%	±5%

Note: *These are theoretical values provided for reference only. Actual values may vary depending on the actual process.*

6.14 Power-on Considerations

No microcontroller is guaranteed to operate properly before the power supply stabilizes to a steady state. The EM88F712N is equipped with a built-in Power-On Voltage Detector (POVD) with a detect level of 2.0V. It will work well if VDD rises fast enough (0.05V/ms or less). However, in many critical applications, extra devices are still required to assist in solving power-up problems.

6.15 External Power-on Reset Circuit

The circuits shown in Figure 6-32 implement an external RC to generate a reset pulse. The pulse width (time constant) should be kept long enough for VDD to reach the minimum operating voltage. Apply this circuit when the power supply has a slow rising time. Since the current leakage from the /RESET pin is about ±5 µA, it is recommended that R should not be greater than 40 KΩ in order for the /RESET pin voltage to remain below 0.2V. The diode (D) acts as a short circuit at the moment of power-down. The capacitor (C) will discharge rapidly and fully. The current-limited resistor (Rin) will prevent high current or ESD (electrostatic discharge) from flowing to Pin /RESET.

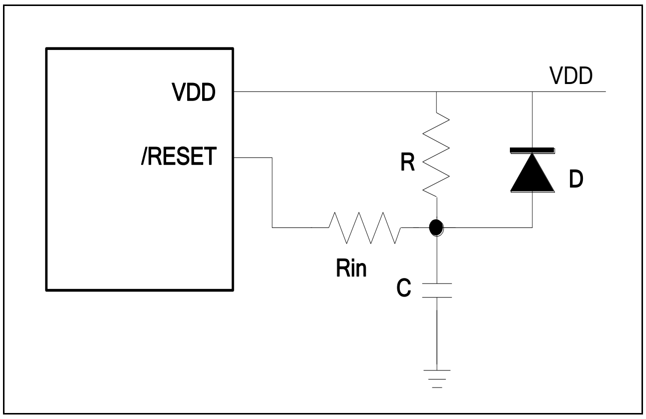


Figure 6-32 External Power-up Reset Circuit

6.16 Residue-Voltage Protection

When the battery is replaced, device power (VDD) is taken off but residue-voltage remains. The residue-voltage may trip below VDD minimum, but not to zero. This condition may cause a poor power-on reset. Figures 6-33a and 6-33b show how to build and accomplish a proper residue-voltage protection circuit.

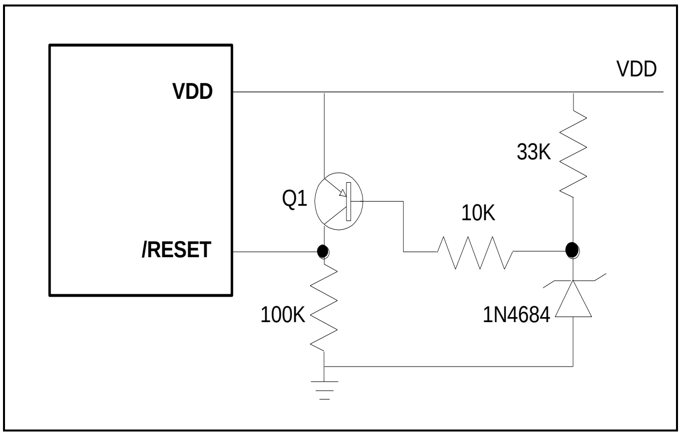


Figure 6-33a Residue Voltage Protection Circuit 1

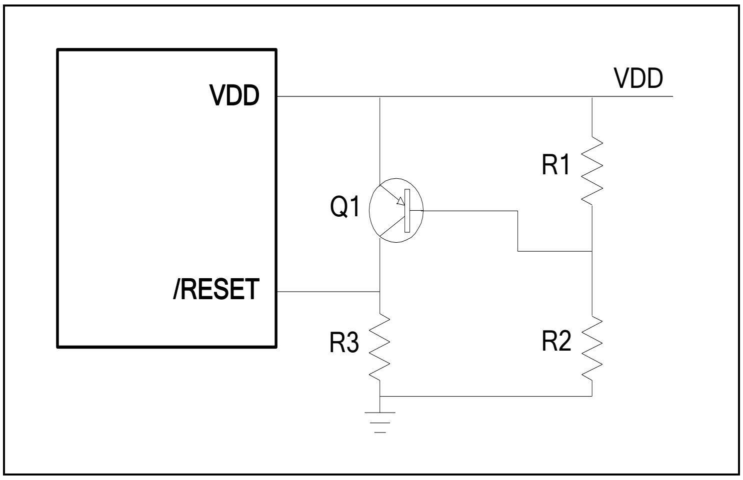


Figure 6-33b Residue Voltage Protection Circuit 2

6.17 Code Option

6.17.1 Code Option Register (Word 0)

Word 0								
	Bit 15	Bit 14	Bit 13	Bit 12	Bit11	Bit10	Bit9	Bit8
Mnemonic	-	-	-	IODG1	IODG0	HLFS	HLP	LVR1
1	High	High	High	High	High	Green	Low PWR	High
0	Low	Low	Low	Low	Low	Normal	High PWR	Low
Default	0	0	0	0	0	0	0	0
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Mnemonic	LVR0	RESETEN	ENWDT	NRHL	NRE	-	-	-
1	High	/RST	Enable	8/fc	Disable	High		
0	Low	P81	Disable	32/fc	Enable	Low		
Default	0	0	0	0	0	0		

Bits 15~13: Not used, set to "0" all the time.

Bits 12~11 (IODG1~IODG0): SPI/UART pin deglitch time select bits.

IODG1~0	UART pin deglitch time	SPI pin deglitch time
00	50ns@5v, Typical (default)	Typical delay = 8ns
01	200ns@5v, Typical	Typical delay = 15ns
10	400ns@5v, Typical	Typical delay = 25ns
11	no deglitch	no deglitch

Bit 10 (HLFS): Reset to Normal or Green Mode Select Bit

1: CPU is selected as Green mode when a reset occurs.

0: CPU is selected as Normal mode when a reset occurs. (default)

Bit 9 (HLP): Power Consumption Selection

1: Low power consumption, apply to working frequency at 1MHz or below 1MHz

0: High power consumption, apply to working frequency above 1MHz

Bits 8~7 (LVR1~LVR0): Low Voltage Reset enable bit.

LVR1, LVR0	*VDD Reset Level	VDD Release Level
00	NA (Power on reset) (default)	
01	2.5V	2.7V
10	3.5V	3.7V
11	4.0V	4.2V

Note: If VDD < 2.7V and remains for about 5us, IC will be reset.
If VDD < 3.7V and remains for about 5us, IC will be reset.
If VDD < 4.2V and remains for about 5us, IC will be reset.

Bit 6 (RESETEN): P81/RESET pin selection bit

1: Enable, P81 as RESET pin.

0: Disable, P81 as I/O pin (default)

Bit 5 (ENWDT): WDT enable bit

1: Enable

0: Disable (default)

Bit 4 (NRHL): Noise rejection high/low pulse define bit.

1: pulses equal to 8/Fc [s] is regarded as signal

0: pulses equal to 32/Fc [s] is regarded as signal (default)

<Note> In Low XTAL oscillator (LXT) mode the noise rejection high/low pulses always 8/Fm.

Bit 3 (NRE): Noise rejection enable bit

1: Disable.

0: Enable (default). **But in Green, Idle, and Sleep modes, the noise rejection circuit is always disabled.**

Bits 2~0: Not used, set to "0" all the time.

6.17.2 Code Option Register (Word 1)

Word 1								
	Bit 15	Bit 14	Bit 13	Bit 12	Bit11	Bit10	Bit9	Bit8
Mnemonic	-	-	FSS	-	-	-	-	-
1	High	High	High	High	High	High	High	High
0	Low	Low	Low	Low	Low	Low	Low	Low
Default	0	0	0	0	0	0	0	0
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Mnemonic	-	RCM2	RCM1	RCM0	OSC2	OSC1	OSC0	-
1	High	High	High	High	High	High	High	High
0	Low	Low	Low	Low	Low	Low	Low	Low
Default	0	0	0	0	0	0	0	0

Bits 15~14: Not used, set to "0" all the time.

Bit 13 (FSS): Sub-oscillator mode selection bits

0: 16kHz (WDT frequency)

1: 128kHz.

Bits 12~7: Not used, set to "0" all the time.

Bits 6~4 (RCM2~RCM0): IRC frequency selection.

* Corresponding with control register Bank0 RE RCM2~RCM0

RCM2	RCM1	RCM0	Frequency (MHz)
0	0	0	4(default)
0	0	1	1
0	1	0	8
0	1	1	10
1	0	0	12
1	0	1	16
1	1	0	20
1	1	1	Reserved

Bits 3~1 (OSC2~OSC0): Main-oscillator mode selection bits.

Main-oscillator mode	OSC2	OSC1	OSC0
IRC (Internal RC oscillator mode) (default) RCOUT (P51) acts as I/O pin	0	0	0
IRC (Internal RC oscillator mode) RCOUT (P51) acts as clock output pin	0	0	1
HXT1 (High XTAL1 oscillator mode) Frequency range: 12~20MHz	0	1	0
HXT2(High XTAL2 oscillator mode) Frequency range: 6~12MHz	0	1	1
XT (XTAL oscillator mode) Frequency range: 1~6MHz	1	0	0
LXT1 (Low XTAL1 oscillator mode) Frequency range: 100K~1MHz	1	0	1
Reserve	1	1	X

Bit 0: Not used, set to "0" all the time.

6.17.3 Code Option Register (Word 2)

Word 2								
	Bit 15	Bit 14	Bit 13	Bit 12	Bit11	Bit10	Bit9	Bit8
Mnemonic	-	SHEN	SHCLK1	SHCLK0				
1	High	Disable	High	High				
0	Low	Enable	Low	Low				
Default	0	0	0	0	0	0	0	0
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Mnemonic	IRCPSS	-	-		-	-	-	-
1	VDD	-	-		-	-	-	-.
0	Int. Vref	-	-		-	-	-	-
Default	0	0	0	0	0	0	0	0

Bit 15: Not used, set to "0" all the time.

Bit 14 (SHEN): System hold enable bit.

1: Disable

0: Enable

Bits 13~12 (SHCLK1~SHCLK0): System hold clock selection bits (extra 128 kHz source)

SHCLK1~0	System hold clock
00	8 clocks (default)
01	4 clocks
10	16 clocks
11	32 clocks

Bits 11~8: Not used, set to "0" all the time.

Bit 7 (IRCPSS): IRC Power Source Selection

1: VDD

0: Internal reference (default)

Bits 6~0: Not used, set to "0" all the time.

6.17.4 Code Option Register (Word 3)

Word 3								
	Bit 15	Bit 14	Bit 13	Bit 12	Bit11	Bit10	Bit9	Bit8
Mnemonic	-	EFTIM	-	-	ADFM	-	-	IRCOMS
1	High	Heavy	High	High	High	High	High	Slowdown
0	Low	Light	Low	Low	Low	Low	Low	Speedup
Default	0	0	0	0	0	0	0	0
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Mnemonic	RLEN		ID5	ID4	ID3	ID2	ID1	ID0
1	Reload	High	Customer ID					
0	No Reload	Low						
Default	0	0						

Bit 15: Not used, set to "0" all the time.

Bit 14 (EFTIM): Low Pass Filter (0: heavy, 1: light)

1: Pass ~ 10MHz (heavy LPS)

0: Pass ~ 25MHz (light LPS) (default)

Bits 13~12: Not used, set to "0" all the time.

Bit 11 (ADFM): This bit controls the format of AD data buffer (ADDH & ADDL). Refer to the following table.

ADFM			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
12 bits	0	ADDH					ADD11	ADD10	ADD9	ADD8
		ADDL	ADD7	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0
	1	ADDH	ADD11	ADD10	ADD9	ADD8	ADD7	ADD6	ADD5	ADD4
		ADDL					ADD3	ADD2	ADD1	ADD0

Note: *Do not use if the hardware bits are set to “**0**”.*

If ADFM=0, ADDH<7:4> = 0000.

Bits 10~9: Not used, set to "0" all the time.

Bit 8 (IRCOMS): IRC Oscillation Mode Select bit (**Not for Customer**).

1: IRC oscillation frequency is slowed down to the setting value.

0: IRC oscillation frequency is speeded up to the setting value. (Default)

Maximum Operating Speed

VDD	IRCOMS=0 Fxt max. (MHz)	IRCOMS=1 Fxt max. (MHz)
2.2	8.0	4.0
3.3	16.0	10.0
5.0	20.0	12.0

Bit 7 (RLEN): Reload Enable

1: Program code reloaded

0: No reload function

Bit 6: Not used, set to "0" all the time.

Bits 5~0 (ID5~ID0): Customer's ID Code

6.17.5 Code Option Register (Word D)

Word D								
	Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit11**	**Bit10**	**Bit9**	**Bit8**
Mnemonic			**SC5**	**SC4**	**SC3**	**SC2**	**SC1**	**SC0**
1	High	High	High	High	High	High	High	High
0	Low	Low	Low	Low	Low	Low	Low	Low
Default	0	0	0	0	0	0	0	0
	Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Mnemonic		**C6**	**C5**	**C4**	**C3**	**C2**	**C1**	**C0**
1	High	High	High	High	High	High	High	High
0	Low	Low	Low	Low	Low	Low	Low	Low
Default	0	0	0	0	0	0	0	0

Bits 15~14: Not used, set to "0" all the time.

Bits 13~8 (SC5~SC0): Trim bits of sub frequency IRC. These are automatically set by writer and eUIDE II.

Bit 7: Not used, set to "0" all the time.

Bits 6~0 (C6~C0): IRC trim bits. These are automatically set by writer and eUIDE II.

6.18 Instruction Set

Each instruction in the instruction set is a 15-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of 2 oscillator periods), unless the program counter is changed by instruction "MOV R2,A", "ADD R2,A", or by instructions of arithmetic or logic operation on R2 (e.g. "SUB R2,A", "BS(C) R2,6", "CLR R2", etc.). In this case, the execution takes two instruction cycles.

If for some reasons, the specification of the instruction cycle is not suitable for certain applications, try modifying the instruction as follows:

The conditional skip ("JBS", "JBC", "JZ", "JZA", "DJZ", "DJZA") commands which were tested to be true, are executed within two instruction cycles. The instructions that are written to the program counter also take two instruction cycles.

In addition, the instruction set has the following features:

(1) Every bit of any register can be set, cleared, or tested directly (except read-only)

(2) The I/O register can be regarded as general register. That is, the same instruction can operate on I/O register.

- **Instruction Set Convention:**

R = *Register designator that specifies which one of the registers (including operation and general-purpose registers) is to be utilized by the instruction.*

b = *Bit field designator that selects the value for the bit located in the register R and which affects the operation.*

k = *8 or 12-bit constant or literal value*

Mnemonic	Operation	Status Affected
NOP	No Operation	None
DAA	Decimal Adjust A	C
SLEP	0 → WDT, Stop oscillator	T,P
WDTC	0 → WDT	T,P
ENI	Enable Interrupt	None
DISI	Disable Interrupt	None
RET	[Top of Stack] → PC	None
RETI	[Top of Stack] → PC, Enable Interrupt	None
RESET	Software Device Reset	ALL Registers = Reset Value Flags* = Reset Value
INT k	PC+1 → [SP], k*2 → PC	None
BTG R,b	Bit Toggle R ; /(R<b>)->R<b> *Range R0~RF	None
MOV R,A	A → R	None
CLRA	0 → A	Z
CLR R	0 → R	Z
SUB A,R	R-A → A	Z, C, DC

Mnemonic	Operation	Status Affected
SUB R,A	R-A → R	Z, C, DC
DECA R	R-1 → A	Z
DEC R	R-1 → R	Z
OR A,R	A ∨ R → A	Z
OR R,A	A ∨ R → R	Z
AND A,R	A & R → A	Z
AND R,A	A & R → R	Z
XOR A,R	A ⊕ R → A	Z
XOR R,A	A ⊕ R → R	Z
ADD A,R	A + R → A	Z, C, DC
ADD R,A	A + R → R	Z, C, DC
MOV A,R	R → A	Z
MOV R,R	R → R	Z
COMA R	/R → A	Z
COM R	/R → R	Z
INCA R	R+1 → A	Z
INC R	R+1 → R	Z
DJZA R	R-1 → A, skip if zero	None
DJZ R	R-1 → R, skip if zero	None
RRCA R	R(n) → A(n-1), R(0) → C, C → A(7)	C
RRC R	R(n) → R(n-1), R(0) → C, C → R(7)	C
RLCA R	R(n) → A(n+1), R(7) → C, C → A(0)	C
RLC R	R(n) → R(n+1), R(7) → C, C → R(0)	C
SWAPA R	R(0-3) → A(4-7), R(4-7) → A(0-3)	None
SWAP R	R(0-3) ↔ R(4-7)	None
JZA R	R+1 → A, skip if zero	None
JZ R	R+1 → R, skip if zero	None
BC R,b	0 → R(b)	None
BS R,b	1 → R(b)	None
JBC R,b	if R(b)=0, skip	None
JBS R,b	if R(b)=1, skip	None
CALL k	PC+1 → [SP], (Page, k) → PC	None
JMP k	(Page, k) → PC	None
MOV A,k	k → A	None
JE R	Compare R with ACC, Skip =	None
JGE R	Compare R with ACC, Skip >	None
JLE R	Compare R with ACC Skip <	None
OR A,k	A ∨ k → A	Z
JE k	Compare K with ACC, Skip =	None
TBRDA R	ROM[(TABPTR)] → R, A A ← program code (low byte) ; R ← program code (high byte)	None
AND A,k	A & k → A	Z
SJC k	Jump to K if Carry *Range [Address±128]	None
SJNC k	Jump to K if Not Carry *Range [Address±128]	None
SJZ k	Jump to K if Zero	None

Mnemonic	Operation	Status Affected
	*Range [Address±128]	
XOR A,k	A ⊕ k → A	Z
SJNZ k	Jump to K if Not Zero *Range [Address±128]	None
RRA R	R(n) → A(n-1), R(0) → A(7)	N
RR R	R(n) → R(n-1), R(0) → R(7)	N
RETL k	k → A, [Top of Stack] → PC	None
XCH R	R ⟷ A	None
RLA R	R(n) → A(n+1), R(7) → A(0)	N
RL R	R(n) → R(n+1), R(7) → R(0)	N
SUB A,k	k-A → A	Z, C, DC
SUBB A,R	R-A-/C → A	Z, C, DC, OV, N
SUBB R,A	R-A-/C → R	Z, C, DC, OV, N
SBANK k	K->R1(4)	None
GBANK k	K->R1(0)	None
TBRD R	ROM[(TABPTR)] → R	None
ADD A,k	k+A → A	Z, C, DC
NEG R	2's complement, /R +1 → R	Z,C,DC,OV,N
ADC A,R	A+R+C → A	Z,C,DC,OV,N
ADC R,A	A+R+C → R	Z,C,DC,OV,N

7 Absolute Maximum Ratings

Items	Rating		
Temperature under bias	-40°C	to	85°C
Storage temperature	-65°C	to	150°C
Input voltage	VSS-0.3V	to	VDD+0.5V
Output voltage	VSS-0.3V	to	VDD+0.5V
Operating Voltage	2.2V	to	5.5V
Operating Frequency	DC	to	20 MHz

8 DC Electrical Characteristics

VDD=5.0V, VSS=0V, Ta=25°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Fxt	XTAL: VDD to 3V	Two cycles with two clocks	DC	8	–	MHz
	XTAL: VDD to 5V		DC	16	–	MHz
	IRC: VDD to 5V	4 MHz, 1 MHz, 8kHz, 10MHz, 12MHz, 16 MHz, 20MHz,	–	F	–	Hz
	IRC: VDD=5V, 25°C	Use UWTR/ NUWTR	-2	F	+2	%
IIL	Input Leakage Current for input pins	VIN = VDD, VSS	-1	0	1	μA
IRCE	Internal RC oscillator error per stage	–	–	±1	–	%
IRC1	IRC:VDD to 5V	RCM2~RCM1=000		4		MHz
IRC2	IRC:VDD to 5V	RCM2~RCM1=001		1		MHz
IRC3	IRC:VDD to 5V	RCM2~RCM1=010		6		MHz
IRC4	IRC:VDD to 5V	RCM2~RCM1=011		8		MHz
IRC5	IRC:VDD to 5V	RCM2~RCM1=100		12		MHz
IRC6	IRC:VDD to 5V	RCM2~RCM1=101		16		MHz
IRC7	IRC:VDD to 5V	RCM2~RCM1=110		20		MHz
VIH1	Input High Voltage (Schmitt Trigger)	Ports 5, 6, 8	0.7VDD	–	VDD+0.3V	V
VIL1	Input Low Voltage (Schmitt Trigger)	Ports 5, 6, 8	-0.3V	–	0.3VDD	V
VIHT1	Input High Threshold Voltage (Schmitt Trigger)	/RESET	0.7VDD	–	VDD+0.3V	V
VILT1	Input Low Threshold Voltage (Schmitt Trigger)	/RESET	-0.3V	–	0.3VDD	V
VIHT2	Input High Threshold Voltage (Schmitt Trigger)	INT	0.7VDD	–	VDD+0.3V	V
VILT2	Input Low Threshold Voltage (Schmitt Trigger)	INT	-0.3V	–	0.3VDD	V
VIHX1	Clock Input High Voltage	OSCI in crystal mode	2.9	3.0	3.1	V
VILX1	Clock Input Low Voltage	OSCI in crystal mode	1.7	1.8	1.9	V
IOH1	Output High Voltage (Ports 5~8)	VOH = VDD-0.1VDD	-3	-5	–	mA
IOH2	Output High Voltage(Hi Drive) (Ports 5~8)	VOH = VDD-0.1VDD	-6	-10	–	mA
IOL1	Output Low Voltage (Ports 5~8)	VOL = GND+0.1VDD	6.8	12	–	mA
IOL2	Output Low Voltage(Hi Sink) (Ports 5~8)	VOL = GND+0.1VDD	16	28	–	mA
IPH	Pull-high current	Pull-high active, input pin @ VSS	-50	-70	-90	μA
IPL	Pull-low current	Pull-low active, input pin @ VDD	20	40	60	μA

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
LVR1	Low voltage reset Level 1 (2.3V)	Ta = 25°C	2.1	2.3	2.51	V
		Ta = -40°C ~ 85°C	2.0	2.3	2.64	V
LVR2	Low voltage reset Level 2 (3.3V)	Ta = 25°C	3.05	3.3	3.55	V
		Ta = -40°C ~ 85°C	2.9	3.3	3.72	V
LVR3	Low voltage reset Level 3 (3.8V)	Ta = 25°C	3.51	3.8	4.11	V
		Ta = -40°C ~ 85°C	3.28	3.8	4.29	V
ISB1	Power down current (Sleep mode)	Ta=25°C, /RESET= 'High', Fm & Fs off All input and I/O pins at VDD, Output pin floating, WDT disabled, IIPS=1	–	1	2	μA
		Ta=85°C, /RESET= 'High', Fm & Fs off All input and I/O pins at VDD, Output pin floating, WDT disabled IIPS=1	–	1.5	2.5	μA
ISB2	Power down current (Sleep mode)	IIPS=1, /RESET= 'High', Fm & Fs off All input and I/O pins at VDD, output pin floating, WDT enabled	–	9.5	11.4	μA
ISB3	Power down current (Sleep mode)	IIPS=0, /RESET= 'High', Fm & Fs off All input and I/O pins at VDD, output pin floating, WDT disabled	–	19	22.8	μA
ISB4	Power down current (Idle mode)	/RESET= 'High', Fm off, Fs on (IRC type), output pin floating, WDT enabled, IRCPSS=1	–	29	34.8	μA
ISB5	Power down current (Idle mode)	/RESET= 'High', Fm=4MHz (IRC type), Fs on (IRC type) output pin floating, WDT enabled, IRCPSS=1	–	160	192	μA
		/RESET= 'High', Fm=4MHz (IRC type), Fs on (IRC type), output pin floating, WDT enabled, IRCPSS=0	–	500	600	μA
ISB6	Power down current (Idle mode)	/RESET= 'High', Fm=4MHz (Crystal type) , Fs on (IRC type), output pin floating, WDT enabled,	–	530	636	μA
ICC1	Operating supply current (Green mode)	/RESET= 'High', Fm off, Fs=16kHz (IRC type), output pin floating, WDT enabled	–	32	38.4	μA
ICC2	Operating supply current (Green mode)	/RESET= 'High', Fm off, Fs=128kHz (IRC type), Output pin floating, WDT enabled	–	68	81.6	μA
ICC3	Operating supply current (Normal mode)	/RESET= 'High', Fm=4 MHz (IRC type), Fs on, output pin floating, WDT enabled	–	1.4	1.68	mA
ICC4	Operating supply current (Normal mode)	/RESET= 'High', Fm=4 MHz (Crystal type), Fs on, output pin floating, WDT enabled	–	1.8	2.16–	mA
ICC5	Operating supply current (Normal mode)	/RESET= ‘High’, Fm=16 MHz (IRC type), Fs on, output pin floating, WDT enabled	–	4.3	5.16	mA
ICC6	Operating supply current (Normal mode)	/RESET= ‘High’, Fm=16 MHz (Crystal type), Fs on, output pin floating, WDT enabled	–	3.8	4.56	mA

*** These parameters are characterized but not tested.**
**** Data in the Minimum, Typical, and Maximum (“Min.”, “Typ.”, “Max.”) columns are based on characterization results at 25°C. These data are for design reference only and have not been tested.**

8.1 AD Converter Characteristics

VDD=5V, VSS=0V, Ta=25°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{AREF}	Analog reference voltage	V_{AREF}-V_{ASS} ≧ 2.5V	2.5	–	VDD	V
V_{ASS}			VSS	–	VSS	V
VAI	Analog input voltage	–	V_{ASS}	–	V_{AREF}	V
IAI1 Ivdd	Analog supply current	V_{AREF} = VDD = 5.5V V_{ASS} = VSS = 0V FS=100kHz, FIN=1kHz (VREF is internal VDD)	–	–	1000	μA
IAI1 Ivref			–	–	10	μA
IAI2 Ivdd	Analog supply current	V_{AREF} = VDD = 5.5V V_{ASS} = VSS = 0V FS=100kHz, FIN=1kHz (VREF is external VREF pin)	–	–	600	μA
IAI2 Ivref			–	–	400	μA
INL	Integral nonlinearity	V_{AREF} = VDD = 5V V_{ASS} = VSS = 0V FS=100kHz, FIN=1kHz	–	–	±4	LSB
DNL	Differential nonlinear	V_{AREF} = VDD = 5V V_{ASS} = VSS = 0V FS=100kHz, FIN=1kHz	–	–	±1	LSB
FSE	Full scale error	V_{AREF} = VDD = 5V V_{ASS} = VSS = 0V, Fs=100kHz	–	–	±8	LSB
OE	Offset error	V_{AREF} = VDD = 5V V_{ASS} = VSS = 0V, Fs=100kHz	–	–	±4	LSB
ZAI	Recommended impedance of analog voltage source	–	–	–	10	kΩ
TAD	A/D clock duration	VDD = 3V~5.5V V_{ASS} = VSS = 0V, FIN=1kHz	0.5	–	–	μs
		VDD = 2.5V~3V V_{ASS} = VSS = 0V, FIN=1kHz	2	–	–	μs
TSH	Sample and Hold time	VDD = 3V~5.5V V_{ASS} = VSS = 0V	4	–	–	μs
		VDD = 2.5V~3V V_{ASS} = VSS = 0V	16	–	–	μs
TCN	A/D conversion time	VDD = 2.5V~5V V_{ASS} = VSS = 0V	–	Tsh+12TAD	–	TAD
$A_{1/2VDD}$	Accuracy for 1/2VDD	–	–	±2	–	%

Notes:

1. *FS is Sample Rate or conversion rate. FIN is freq. of input test sine wave*
2. *The parameters are theoretical values and have not been tested. Such parameters are for design reference only.*
3. *There is no current consumption when ADC is off other than minor leakage current.*
4. *AD conversion result will not decrease when the input voltage is increased, and there is no missing code.*
5. *These parameters are subject to change without further notice.*

* These parameters are characterized but not tested.

* Data in the Minimum, Typical, Maximum("Min","Typ","Max") column are based on characterization results at 25℃. These data are for design guidance only and have not been tested.

8.2 OP Characteristics

VDD=5V, VSS=0V, Ta=25°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{OS}	Input offset voltage	Vip=0.1V, after trimmed	0	±1	±2	mV
SR	Slew rate	RL=1Meg, CL=20p, $V_{I(pp)}$=3V, Av=1	2	2.5		V/us
IVR*	Input voltage range*		0		3.6	V
VOL	Low-level output voltage	Vip=0V, I_L=100uA, Av=1		10	40	mV
		Vip=0V, I_L=1mA, Av=1		50	200	mV
VOH	High-level output voltage	Vip=2.5V, IL=100uA, Av=2	4.920	4.980		V
		Vip=2.5V, IL=1mA, Av=2	4.600	4.850		V
ISC_L	Output sink current (short circuit current)		5	10		mA
ISC_H	Output source current (short circuit current)		5	10		mA
I_{DD}	Supply current	No load, Vic=0.1V, Av=1		200	250	uA
GBP	Gain bandwidth product	RL=1Meg, CL=20p,	1.2	1.9		MHz

* IVR: Max= Vdda-1.4V

* These parameters are characterized but not tested.

* Data in the Minimum, Typical, Maximum("Min","Typ","Max") column are based on characterization results at 25℃. These data are for design guidance only and have not been tested.

8.3 Comparator Characteristics

VDD=5V, VSS=0V, Ta=25°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{OS}	Input offset voltage	Vip=0.1V, after trimmed	0	±1	±2	mV
IVR*	Input voltage range*		0		3.6	V
I_{DD}	Supply current			100	120	uA
TRS	Response time	Vin=0.1V, (Note[1])		0.5	1	us
TLRS	Large signal response time	Vin=1.8V, (Note[2])		50	100	ns

* IVR: Max= Vdda-1.4V

Note[1]: The response time specified is a 100mV input step with 10mV overdrive.

Note[2]: The response time specified is a 0V~3.6V input step with 1.8V overdrive.

* These parameters are characterized but not tested.

* Data in the Minimum, Typical, Maximum("Min","Typ","Max") column are based on characterization results at 25℃. These data are for design guidance only and have not been tested.

8.4 HLVD Characteristics

VDD=5V, VSS=0V, Ta=25°C

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
IHLVD	HLVD Operation current	HLVD Enable, VDD=5V		9.2	11	µA
ΔV	Detect level variation			±0.15		V
VHYST	Hysteresis		50	100	150	mV
TVREF	VREF stable time	HLVD Enable, VDD=5V		30	60	µs

* These parameters are characterized but not tested.
* Data in the Minimum, Typical, Maximum("Min","Typ","Max") column are based on characterization results at 25℃. These data are for design guidance only and have not been tested.

8.5 1/2VDD Characteristics

VDD=5V, VSS=0V, Ta=25°C

symbol	parameter	condition	Min.	Typ.	Max.	Unit
VDD	power supply		2.4	5	5.5	V
Ivdda	DC supply current	VDDA=5V		34.72	42	uA
Ipd	power down current			0.001	< 0.1	uA
warn up time for ADC sample	time ready for voltage reference (VREF1_2VDD)	CL=12.8PF (ADC sample loading)		2.8**	4	us
warn up time for TE testing	time ready for voltage reference to TE testing (VREF1_2VDD_PAD)	CL=100PF (TE testing loading)		18**	25	us
VREF1_2VDD	1/2 VDD voltage output		Typ.-1%	(1/2)VDD	Typ.+1%	V

* These parameters are characterized but not tested.
* Data in the Minimum, Typical, Maximum("Min","Typ","Max") column are based on characterization results at 25℃. These data are for design guidance only and have not been tested.

8.6 VREF Characteristics

VDD=5V, VSS=0V, Ta=25°C

symbol	parameter	condition	Min.	Typ.	Max.	Unit
VDD	power supply		2.2		5.5	V
Ivdd	DC supply current	BG_PD=0 VREF_PD=0		250	400	uA
Tresponse	Response time	Trim bit and VREF select setting time		10**	20	us
warn up time	time ready for voltage reference	EN_LPF=0		10	20	us
		EN_LPF=1		1**	1.5	ms
Vref	Voltage reference output		2.02752	2.048	2.06848	V
			2.53404	2.560	2.58560	
			3.04128	3.072	3.10272	
			4.05504	4.096	4.13696	
Vdd_min	Minimum power supply		Vref+0.1	Vref+0.2*		V

- *Vdd_min: can work at (Vref+0.1V), but has a poor PSRR.

* These parameters are characterized but not tested.
* Data in the Minimum, Typical, Maximum(“Min”,“Typ”,”Max”) column are based on characterization results at 25℃. These data are for design guidance only and have not been tested.

Notes:

1. *The parameters are theoretical values and have not been tested. Such parameters are for design reference only.*
2. *These parameters are subject to change without prior notice.*

9 AC Electrical Characteristics

Ta=25°C, VDD=5V ± 5%, VSS=0V

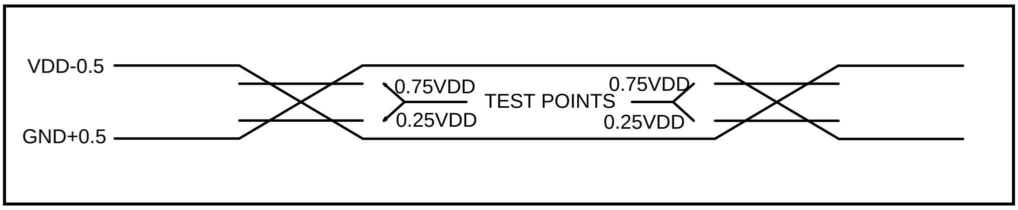
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Dclk	Input CLK duty cycle	–	45	50	55	%
Tins	Instruction Cycle Time	Crystal type	125	–	DC	ns
		IRC type	125	–	DC	ns
Ttcx	TCX Input Period	–	Tins	–	–	ns
Tpor	Delay time after Power-on-Reset release	16kHz	–	16±3%	–	ms
Trstrl	Delay time after /RESET, WDT and LVR release	Crystal type, HLFS=1	–	WSTO+510/Fm	–	–
		IRC type, HLFS=1	–	WSTO+8/Fm	–	–
		Crystal type, HLFS=0	–	WSTO+510/Fs	–	–
		IRC type, HLFS=0	–	WSTO+8/Fs	–	–
Trsth	Hold time after /RESET and LVR reset	–	–	1	–	μs
Twdt	Watchdog timer period	16kHz	–	16±3%	–	ms
Tset	Input pin setup time	–	–	0	–	ns
Thold	Input pin hold time	–	15	20	25	ns
Tdelay	Output pin delay time	Cload=20pF Rload=1M	–	20	–	ns

Note: * ***Tpor*** *and* ***Twdt*** *are16+/- 10% ms at Ta = -40° ~ 85°C, and VDD = 2.1~5.5V*
** **WSTO: Waiting time of Start-to-Oscillation**

1. These parameters are hypothetical (not tested) and are provided for design reference only.
2. Data under Minimum, Typical and Maximum (Min., Typ. and Max.) columns are based on hypothetical results at 25°C. These data are for design reference only and have not been tested or verified.

10 Timing Diagrams

AC Test Input / Output Waveform



Note: *AC Testing**:** Input are driven at VDD-0.5V for logic "**1**," and VSS+0.5V for logic "**0**"*
*Timing measurements are made at 0.75VDD for logic "**1**," and 0.25VDD for logic "**0**"*

Figure 10-1a AC Test Input/Output Waveform Timing Diagram

Reset Timing

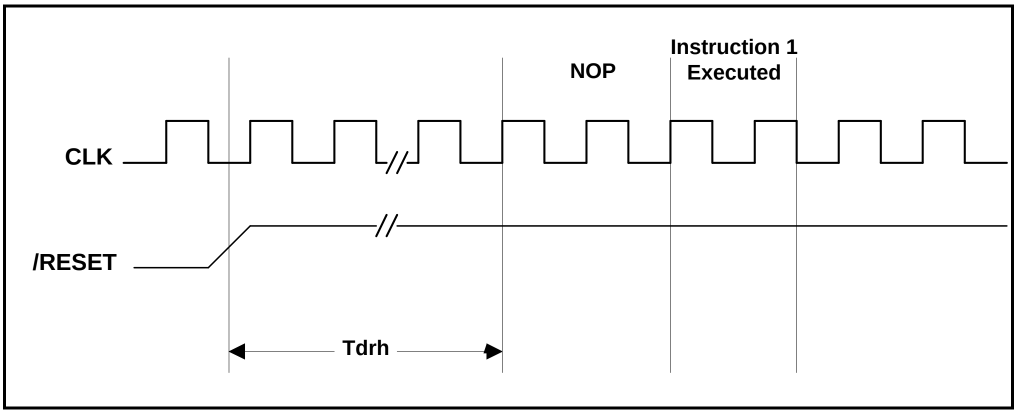


Figure 10-1b Reset Timing Diagram

APPENDIX

A Ordering and Manufacturing Information

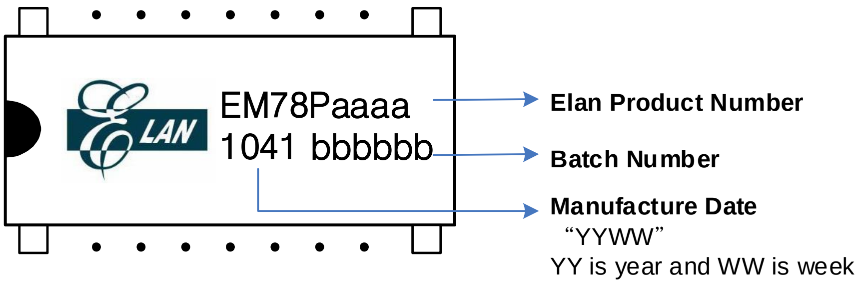
EM88F712NSO20J

- **Material Type**
  J: RoHS complied
  S: Sony SS-00259 complied
  Contact Elan Sales for details
- **Pin Number**
- **Package Type**
  SO: SOP
  SS: SSOP
- **Specific Annotation**
- **Product Number**
- **Product Type**
  F: Flash
- **Elan 8-bit Product**

For example:

EM88F712NSO20J

is EM88F712N with Flash program memory, product, in 20-pin SOP 300mil package with RoHS complied



Ordering Code

EM88F712NSO20J

- **Material Type**
  Contact Elan Sales for details
- **Package Type / Pin Number**
  Check the following section
- **Elan IC Product Number**

B Package Type

Flash MCU	Package Type	Pin Count	Package Size
EM88F712NSO20	SOP	20	300 mil
EM88F712NSS20	SSOP	20	209 mil
EM88F712NSS20A	SSOP	20	150 mil
EM88F712NSO16A	SOP	16	150 mil
EM88F712NSS16	SSOP	16	150 mil

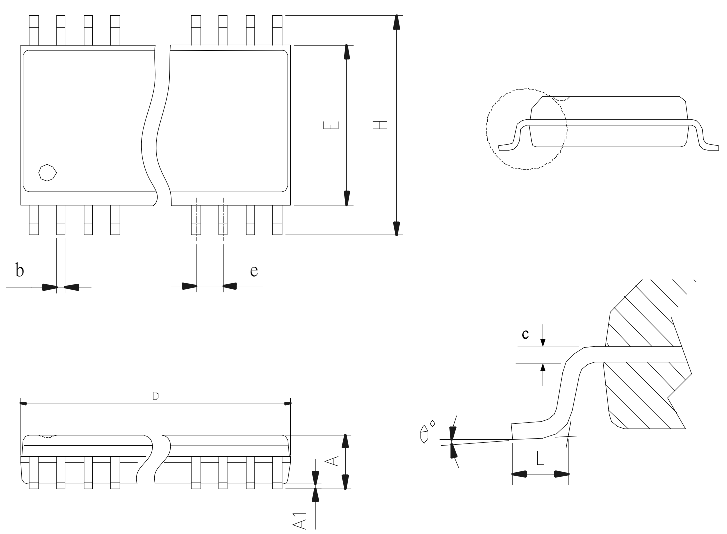
These are Green Products which do not contain hazardous substances and comply with the third edition of Sony SS-00259 standard.

Pb content is less than 100ppm and complies with Sony specifications.

Part No.	EM88F712NxJ / xS
Electroplate type	Pure Tin
Ingredient (%)	Sn:100%
Melting point (°C)	232°C
Electrical resistivity (μΩ-cm)	11.4
Hardness (hv)	8~10
Elongation (%)	>50%

C Package Information

C.1 EM88F712NSO20



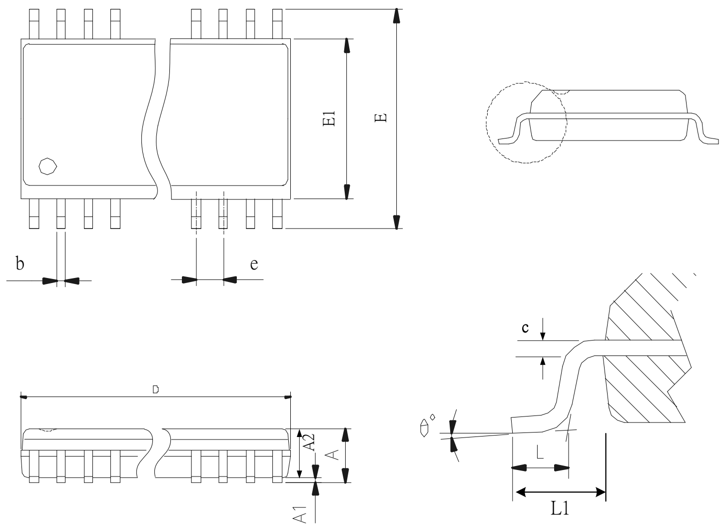
Symbol	Min	Normal	Max
A	2.350		2.650
A1	0.102		0.300
b	0.406(TYP)		
c	0.230		0.320
E	7.400		7.600
H	10.000		10.650
D	12.600		12.900
L	0.630	0.838	1.100
e	1.27(TYP)		
θ°	0		8

TITLE:
SOP-20L(300MIL) PACKAGE OUTLINE DIMENSION

File : SO20	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure C-1 EM88F712N 20-pin SOP Package Type

C.2 EM88F712NSS20

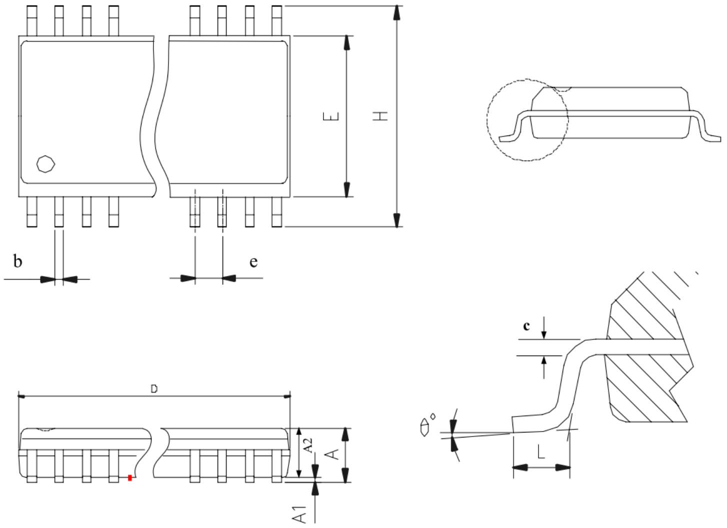


Symbol	Min	Normal	Max
A			2.130
A1	0.050		0.250
A2	1.620	1.750	1.880
b	0.220		0.380
c	0.090		0.200
E	7.400	7.800	8.200
E1	5.000	5.300	5.600
D	6.900	7.200	7.500
L	0.650	0.750	0.850
L1	1.250(REF)		
e	0.650(TYP)		
θ°	0	4	8

TITLE: SSOP-20L(209MIL) OUTLINE PACKAGE PACKA OUTLINE DIMENSION	
File : SSOP20	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure C-2 EM88F712N 20-pin SSOP Package Type

C.3 EM88F712NSO16A

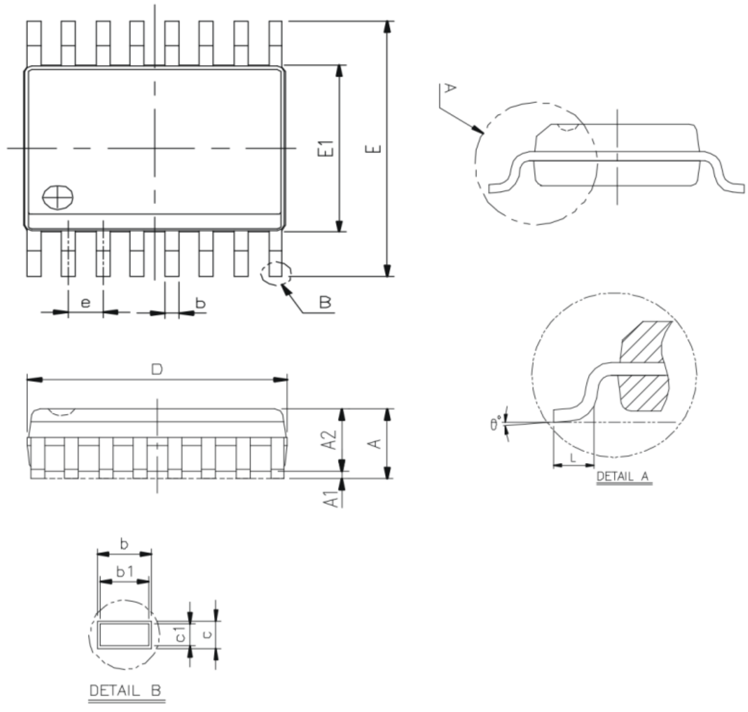


Symbal	Min	Normal	Max
A	1.350		1.750
A1	0.100		0.250
A2	1.300	1.400	1.500
b	0.330		0.510
c	0.190		0.250
E	3.800		4.000
H	5.800		6.200
D	9.800		10.000
L	0.600		1.270
e		1.27(TYP)	
θ°	0		8

TITLE: SOP-16L(150MIL) PACKAGE OUTLINE DIMENSION	
File : NSO16	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure C-3 EM88F712N 16-pin SOP Package Type

C.4 EM88F712NSS16



Package Type : SSOP-16L

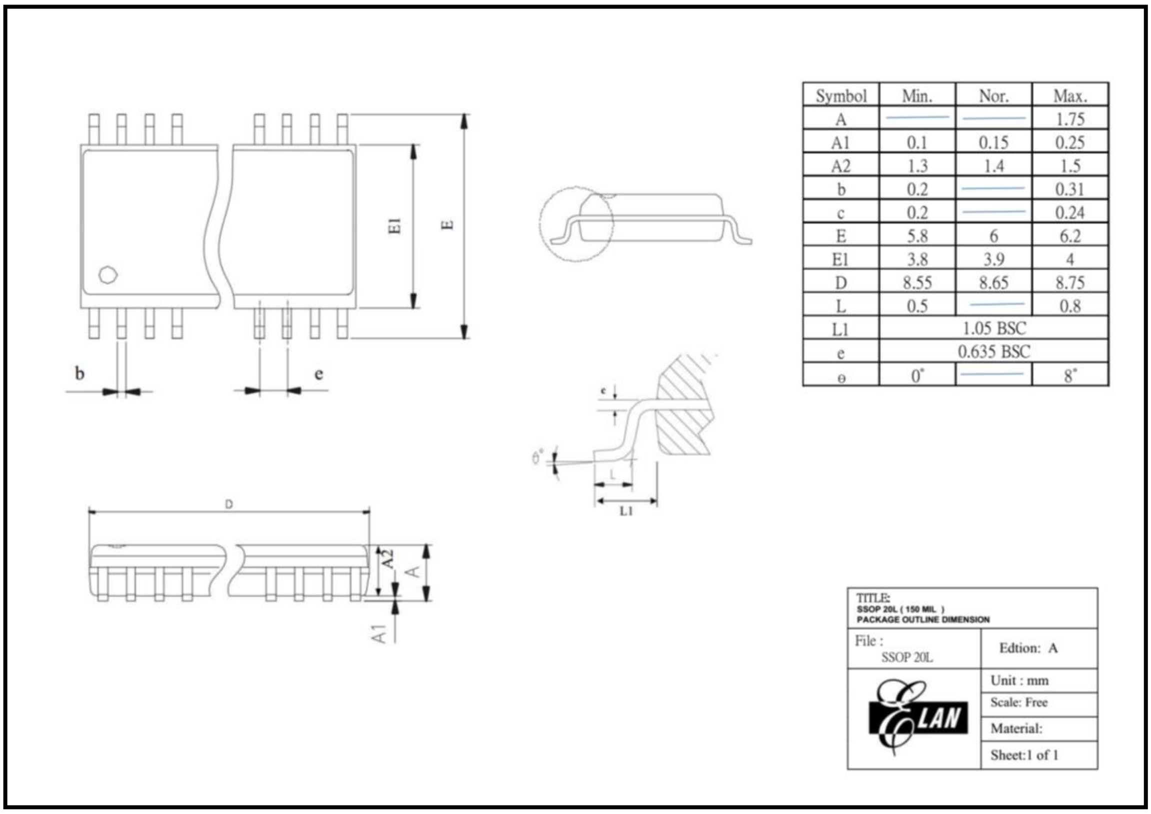
	EMC(mm)		
Symbol	Min	Normal	Max
A	1.35	1.63	1.75
A1	0.10	0.18	0.25
A2	-	-	1.50
b	0.20	-	0.30
b1	0.20	0.25	0.28
c	0.18	-	0.25
c1	0.18	0.20	0.23
D	4.80	4.90	5.00
E	5.79	5.99	6.20
E1	3.81	3.91	3.99
L	0.41	0.64	1.27
e	0.635BASIC		
θ	0°	-	8°

TITLE:
SSOP 16L (150MIL)PACKAGE OUTLINE DIMENSION

File : SSOP 16L	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure C-4 EM88F712N 16-pin SSOP Package Type

C.5 EM88F712NSS20A



Symbol	Min.	Nor.	Max.
A	———	———	1.75
A1	0.1	0.15	0.25
A2	1.3	1.4	1.5
b	0.2	———	0.31
c	0.2	———	0.24
E	5.8	6	6.2
E1	3.8	3.9	4
D	8.55	8.65	8.75
L	0.5	———	0.8
L1	1.05 BSC		
e	0.635 BSC		
θ	0°	———	8°

Figure C-5 EM88F712N 20-pin SSOP Package Type

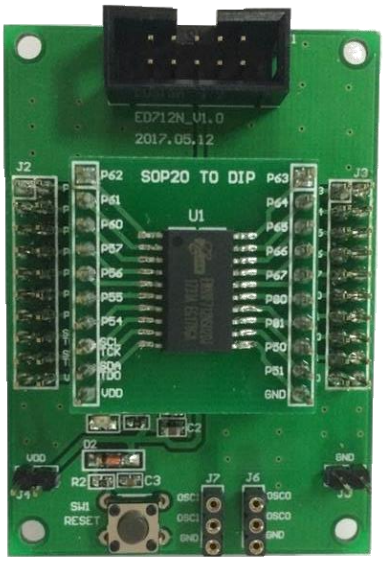
D Quality Assurance and Reliability

Test Category	Test Conditions	Remarks
Solderability	Solder temperature=245±5°C, for 5 seconds up to the stopper using a rosin-type flux	
Pre-condition	Step 1**:** TCT, 65°C (15 min)~150°C (15 min), 10 cycles	For SMD IC (such as SOP, QFP, SOJ, etc.)
	Step 2**:** Bake at 125°C, TD (endurance)=24 hrs	
	Step 3**:** Soak at 30°C/60% , TD (endurance)=192 hrs	
	Step 4**:** IR flow 3 cycles (Pkg thickness ≥ 2.5mm or Pkg volume ≥ 350 mm^3 ----225±5°C) (Pkg thickness ≤ 2.5 mm or Pkg volume ≤ 350 mm^3 ----240±5°C)	
Temperature cycle test	-65°C (15mins)~150°C (15min), 200 cycles	
Pressure cooker test	TA =121°C, RH=100%, pressure = 2 atm, TD (endurance)= 96 hrs	
High temperature / High humidity test	TA=85°C , RH=85% , TD (endurance)=168 , 500 hrs	
High-temperature storage life	TA=150°C, TD (endurance)=500, 1000 hrs	
High-temperature operating life	TA=125°C, VDD=Max. operating voltage, TD (endurance) =168, 500, 1000 hrs	
Latch-up	TA=25°C, VDD=Max. operating voltage, 600mA/40V	
ESD (HBM)	TA=25°C, ≥ | ± 3KV |	IP_ND,OP_ND,IO_ND IP_NS,OP_NS,IO_NS IP_PD,OP_PD,IO_PD, IP_PS,OP_PS,IO_PS, VDD-VSS(+),VDD_VSS (-) mode
ESD (MM)	TA=25°C, ≥ | ± 400V |	

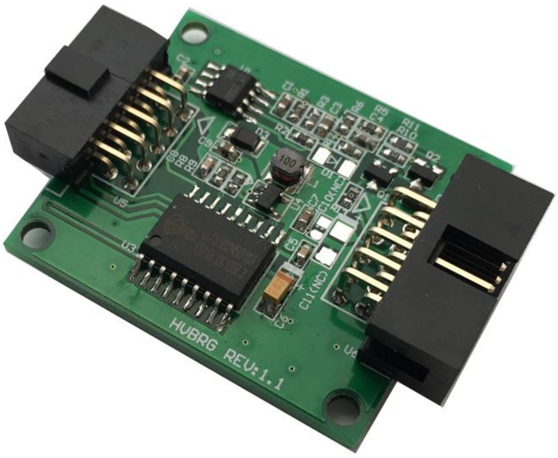
D.1 Address Trap Detect

An address trap detect is one of the MCU embedded fail-safe functions that detects MCU malfunction caused by noise or the like. Whenever the MCU attempts to fetch an instruction from a certain section of ROM, an internal recovery circuit is automatically started. If a noise caused address error is detected, the MCU will repeat execution of the program until the noise is eliminated. The MCU will then continue to execute the next program.

E ED712N & HVBRG & UBRG connection

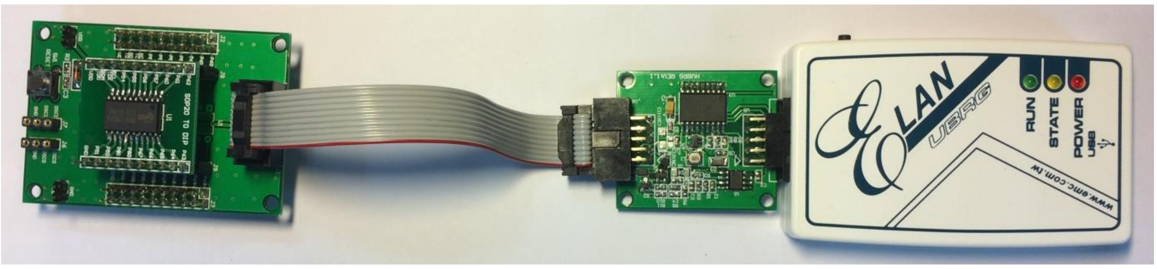


ED712N



HVBRG

UBRG+HVBRG



ED712N+UBRG+HVBRG

> **NOTE**
>
> *When programming EM88F712N (ED712N), the VDD must be 5V for the programming to be successful. Therefore, during EM88F712N programming and ED712N simulation, pay attention to the resistance of the surrounding components.*